D0301-013

RELIABILITY ASSESSMENT

AND

DEVELOPMENT STUDY REPORT

ON

MRIR-PCM SUBSYSTEM

CONTRACT NAS5-9699

Prepared for

Systems Engineering Branch, Code 731
National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland

31 December 1965

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SECTION 1

INTRODUCTION

The MRIR Telemetry Unit Engineering Model, prior to fabrication and testing, has been subjected to a system reliability and developmental analysis.

1.1 SCOPE

This report contains the results of the analysis which was performed by California Computer Products, Inc. The analysis is divided into two parts. The first part provides the reliability assessment of the MRIR System mechanization, and the second part provides data to support the development, fabrication, assembly, and test of the MRIR Telemetry Unit Subsystem.

1.2 AREAS OF CONSIDERATION

The areas of consideration for the reliability assessment can further be divided into two categories: electrical and logical. The electrical analysis encompasses the following:

a. DC/DC Converter

b. A/D Converter

c. Analog Input Gates

The logical analysis involves the overall logic as it was initially presented. This includes timing and controlling functions.

The second part which covers the overall package development study deals with the following areas:

a. Circuit Design

b. Mechanical Design

c. Interface Specifications

d. Test Procedures

1.3 STANDARDS

The conditions by which the reliability analysis and development study has been performed is based on accepted industry standards as well as the experience of CalComp personnel who have worked on the previous MRIR-PCM NIMBUS "C" Telemetry Subsystem.

The analysis of the circuits was based on worst-case conditions at all times. Components were analyzed in conjunction with manufacturer's recommendations. With these conditions in mind, certain areas of the MRIR Telemetry Unit are questionable as to their operating reliably for the full anticipated lifetime of the NIMBUS satellite. Therefore, CalComp's recommendations are based on readily being able to reproduce the MRIR Subsystem to be reliable and accurate.

SECTION 2

ELECTRONIC ANALYSIS

2.1 DC/DC CONVERTER ANALYSIS

The DC/DC Converter schematic has been carefully analyzed to determine areas of potential trouble. As specified in the introduction, the circuits are reviewed with worst-case conditions in mind. In other areas, recommendations are made in order to enhance certain aspects of the DC/DC Converter.

2.1.1 DC/DC CONVERTER CRITICAL AREAS

The areas which CalComp feels represents potential trouble or critical areas are itemized below.

a. In Figure 2-1, transistors Q6 and Q7 are used as rectifiers. The base-to-emitter rating on these transistors is eight volts. Under operating conditions, the base-emitter voltage can go as high as 10.2 volts. This represents a 27.5 percent increase over the manufacturer's recommended operating specification.

b. The 1N3612 diodes used as rectifiers do not have a reverse recovery specification. Rectifiers are usually specified at 60 cps operating from a sine wave source. The frequency of the DC/DC Converter is higher, and the recovery time of the rectifier diodes becomes significant because of the rise time of the square wave source.

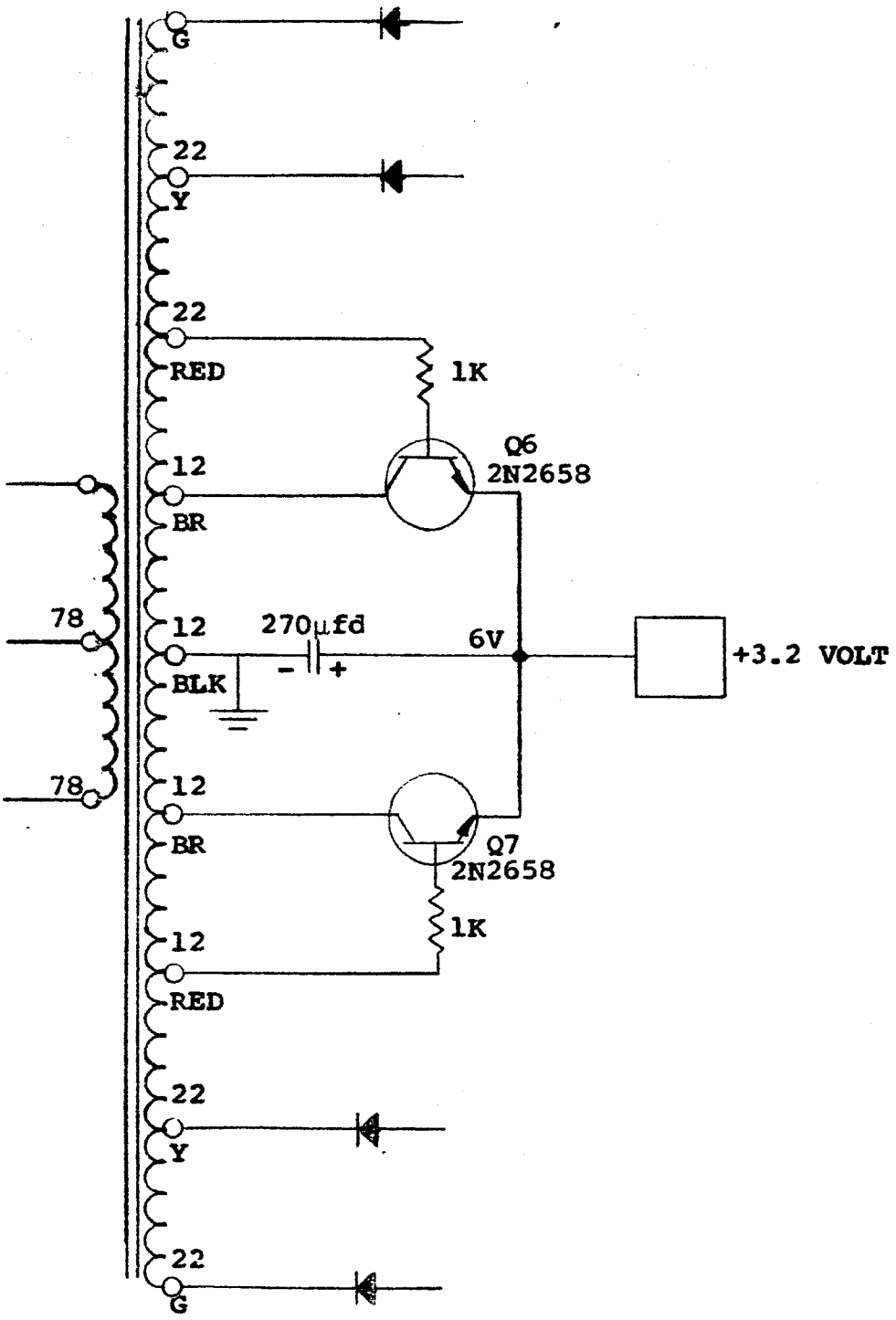


FIGURE 2-1

Transformer and +3.2V Supply

c. The primary voltage input can swing between 0 and -32 volts. The rated working voltage on the input filter capacitors is 35 volts. This voltage swing is very close to the rated working voltage of the capacitor.

d. The output of the secondary voltage levels shows a 10-microhenry inductor in series. This inductance is not sufficient to completely suppress the switching spikes generated in the flux oscillator and secondary rectifiers.

2.1.2 DC/DC IMPROVEMENT AREAS

Other areas in which the operation of the DC/DC Converter is not considered potential trouble areas, but can contribute to a lower reliability or a less readily reproducible DC/DC Converter system, are itemized below.

a. Referring to Figure 2-2, transistor Q5 (2N2927) is used as a reference source by breaking down the base-emitter junction. The replacement of this part makes it selective in order to achieve the same operating characteristics.

b. The h_{fe} for transistors Q1, Q3, and Q4 in Figure 2-3 is specified in the data sheet at a 1-ampere test current. The actual current in this application is in the range of 30 - 100 milliamperes. Gain can be guaranteed only through the selection of transistors.

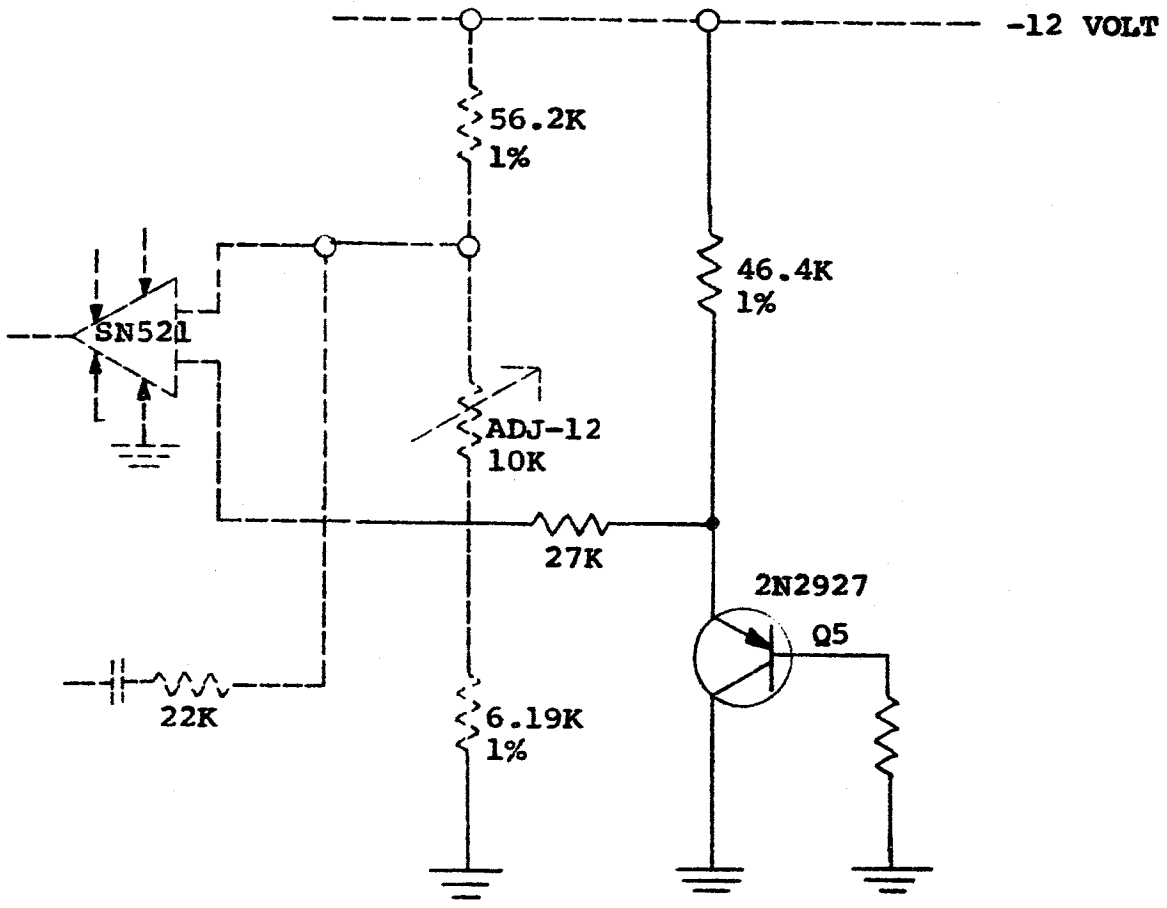


FIGURE 2-2

Temperature Compensation Circuit

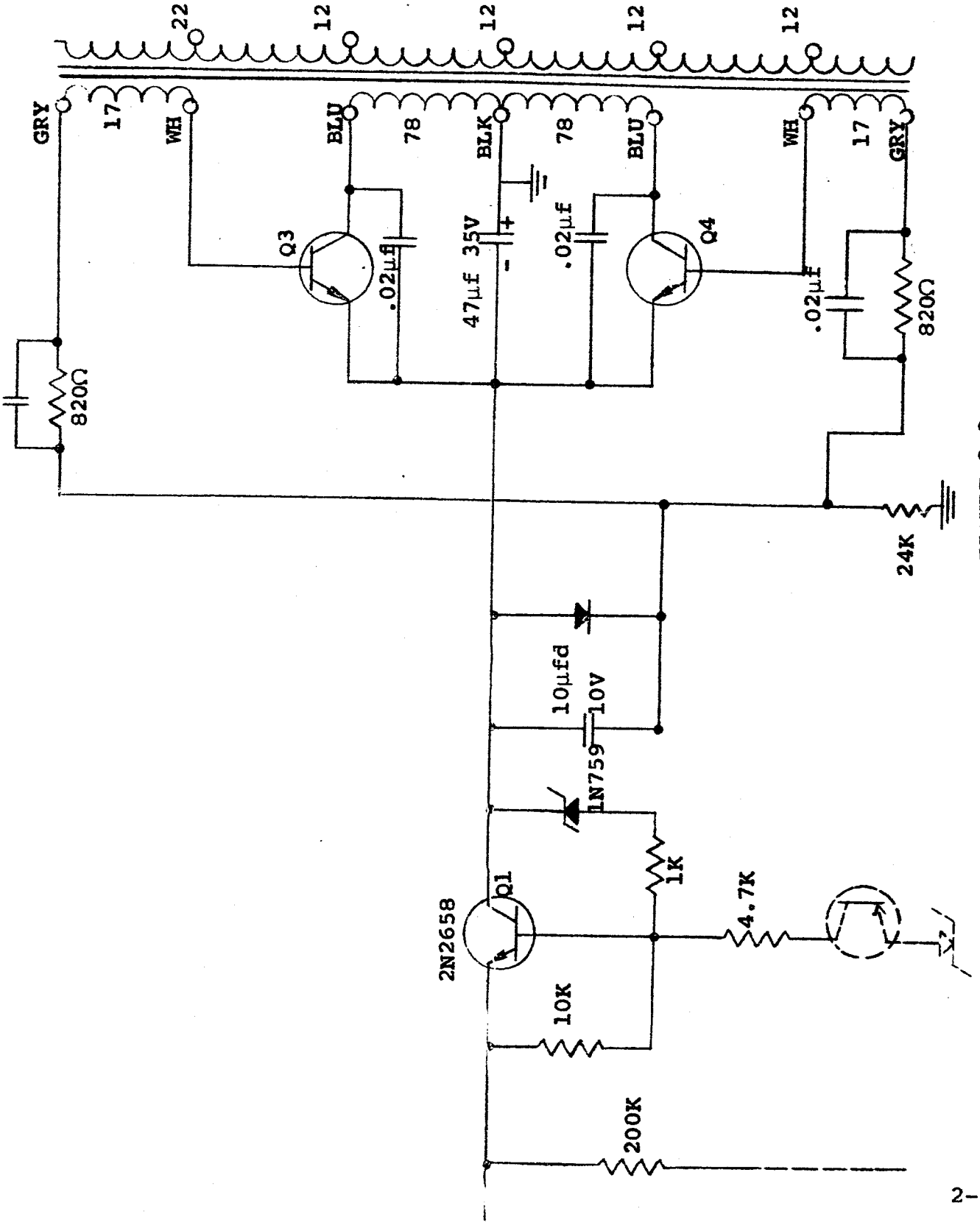


FIGURE 2-3

DC to DC Flux Oscillator

c. The analysis of the transformer has presented two conditions which should be taken into consideration.

(1) The 3.2 volt winding can induce modulation effects on the other windings because of its load changes.

(2) The number of turns on the primary winding is such that any output level can be resolved to within 0.32 volts by either adding or reducing one turn. The +3.2 volt level, which is the most difficult to obtain, is allowed a maximum deviation of ±128 millivolts (±4 percent). If the +3.2 volts is just beyond its outside limits, it could not be resolved into its limits.

d. The operational amplifier which is used as a regulator sensor can exhibit a degree of instability because of its drift characteristics. The higher the input voltage the greater the probability of drift occurrence. Further, the voltage (ground) at pins 3 and 4 is the same. The voltages should be different to provide a more stabilizing bias.

2.2 DC/DC CONCLUSIONS AND RECOMMENDATIONS

Based on the analytical evaluation of the DC/DC Converter schematic MD2154, dated 6 June 1965, it is CalComp's conclusion that the DC/DC Converter is not entirely adequate to meet the full requirements established in the GSFC specification for the MRIR Experiment Telemetry Unit for NIMBUS "B." Since the nature of the evaluation was divided into two categories: (1) potential or critical areas and (2) noncritical areas, the recommendations to bring the DC/DC Converter design up to specification are made in this same categorical relationship. Further, the recommendations made under

critical evaluation are considered to be mandatory to ensure reliable error-free performance.

2.2.1 CRITICAL AREA RECOMMENDATIONS

The recommendations for the critical areas are as follows:

a. Eliminate the Q6 and Q7 rectifier transistors by using diode rectifiers as shown in Figure 2-4 or redesign the 3.2 volt rectifiers so that the emitter-base back voltage will be lower.

b. Use 1N3730 diodes as rectifiers in place of the 1N3612 diodes. The 1N3730 exhibits a good reverse recovery time.

c. The input filter capacitors should be changed to at least a minimum 50-vdc working voltage rating.

d. Additional filtering capacitors should be added at the output of the secondary levels. The LC circuit will ensure the suppression of any spikes generated by the flux oscillator.

2.2.2 IMPROVEMENT RECOMMENDATIONS

The recommendations in support to the second category evaluations are as follows:

a. In place of the Q5 transistor which is used as a reference source, a 1N827A Zener diode should be used. This Zener diode represents more stability and is easily and directly replaceable as it is independent of particular or exact operating characteristics.

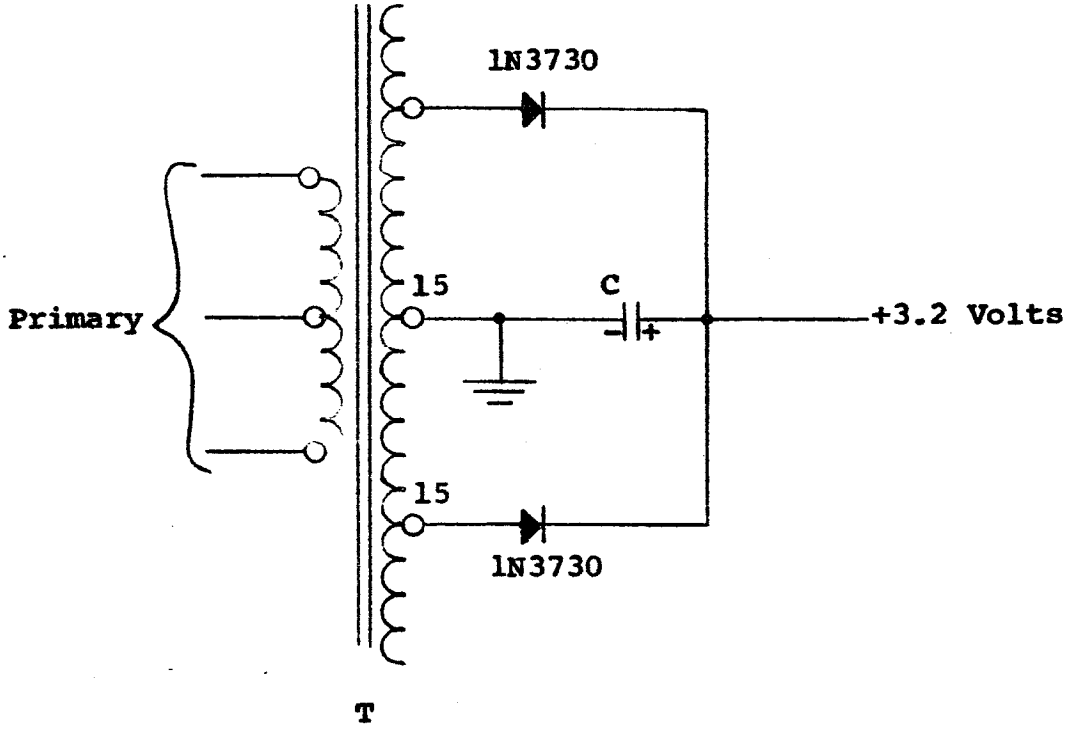


FIGURE 2-4

+3.2V Diode Rectifier

b. The Q1, Q3, and Q4 transistors should be of a type which more closely approaches the manufacturer's recommended operating conditions rather than using a transistor capable of handling 1 ampere to do a 0.1 ampere job.

c. The 3.2 volt winding should be separated from the other levels to reduce the modulation effect of the 3.2 volt load changes. Figure 2-5 shows the new transformer design.

   Since the 3.2 volt tolerance cannot be resolved by the reduction or addition of one primary turn, the tolerance of the 3.2 volt level should be opened up to be equivalent to the resolution of one primary turn, 0.32 volts.

d. To enhance the stability of the operational amplifier which performs the function of overall regulation, it is recommended that the voltage divider input to the amplifier be lowered by a factor of ten and that the potential at pin 4 be changed to +3.2 volts.

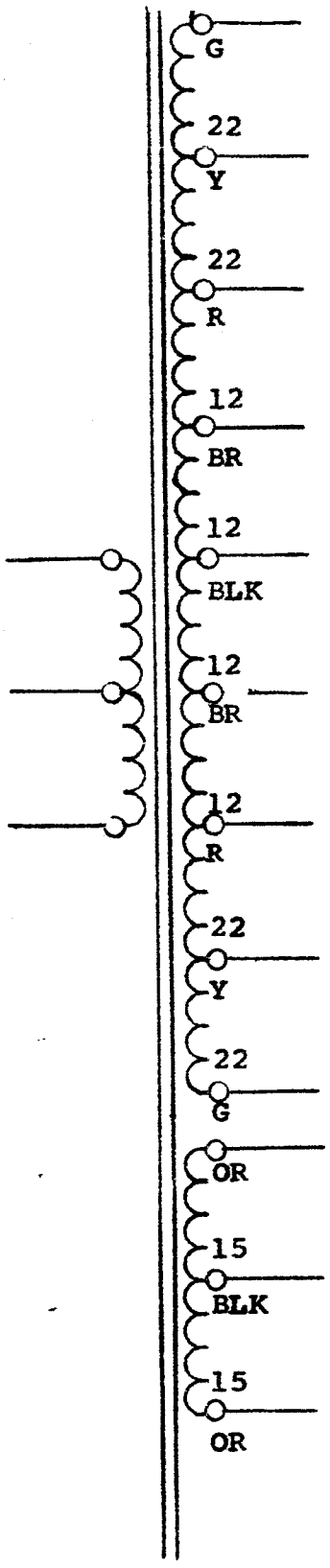


FIGURE 2-5

Transformer Redesign

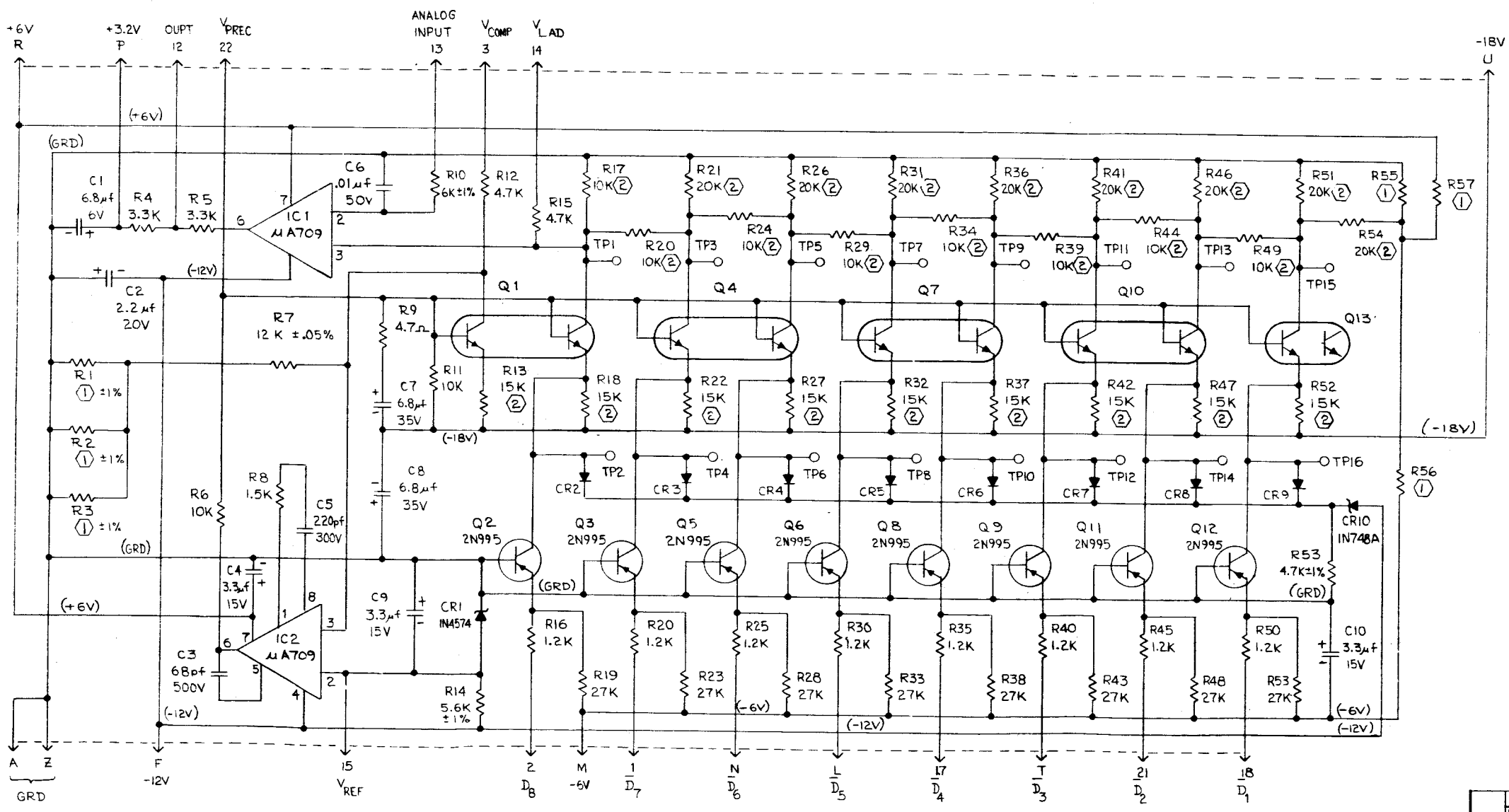
SECTION 3

ANALOG/DIGITAL ELECTRONIC ANALYSIS

The most critical part of the MRIR Telemetry Unit is the analog-to-digital conversion of the Radiometer inputs. The minimum voltage to be resolved is 25 millivolts. The accuracy of this A/D Converter is 1 part out of 256 or 0.375 percent. In order to maintain this accuracy, an evaluation of the A/D schematic has been performed and the reliability assessment of the circuit represented in NASA's drawing MD2165 (C) dated 26 October 1965, is that the potential error contribution of the parts which make up the A/D Converter can exceed the specified tolerance. Further, the design of the A/D Converter places tight restrictions on some parts which makes them rather difficult to obtain. Taking these things into account, CalComp is recommending changes which will keep the error contributions to a minimum thereby guaranteeing the A/D conversion accuracy over the full temperature range, and to make the circuit more reproducible, CalComp recommends that the analog-to-digital conversion circuit be modified as shown in Figure 3-1.

In this circuit, temperature compensation of the current sources is obtained by regulating the current output of a reference transistor. The transistor Q1 in Figure 3-1 is the same type as the ladder current transistors and is operated at the same current. This will make it much easier to match the emitter-base voltages of the transistors to a close tolerance over the expected temperature range. The temperature coefficient of an emitter-base voltage is dependent both on the transistor current and type.

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	



6. REF ASSY DWG NO. 10367-502
5. TRANSISTORS ARE
4. DIODES ARE IN415
(2) 3. VALUES ±0.05% 0.1 W
(1) 2. VALUE TO BE DETERMINED AT FUNCTIONAL TEST
1- RESISTOR VALUES ±2% ¼ W
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	10368-502	SCHEMATIC		

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: XX ± .03, XXX ± .010
ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .128: +.002, —.001
.136 TO .228: +.003, —.001
.234 TO .500: +.004, —.001
.515 TO .750: +.005, —.001
.765 TO 1.000: +.007, —.001
1.015 TO 2.000: +.010, —.001

DRAWN O. HAMPTON 5 Jan 1966
CHECK
APPD
APPD
FINISH
HEAT TREAT
SURFACE ROUGHNESS PER MIL-STD-10 ✓
DO NOT SCALE THIS DRAWING

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC-
ANALOG/DIGITAL CONVERTER

SCALE: NONE
SIZE D
10368-502
WEIGHT
SHEET

FIGURE 3-1

In addition, the reference transistor and the first most significant current source transistor could be a single chip matched pair, ensuring more equal junction temperatures. Subsequent current source transistors could also be single chip pairs.

In the present system, the 2N930 current sources must be matched to each other and to a 2N995 pnp reference transistor which is operated at a much lower and variable current of 0.1 to 0.3 milliampere.

The current for the Zener reference diode (CR1) is supplied by the -12 volt level which is the most closely regulated supply in the system.

R1, R2, and R3 will be adjusted to give the correct full scale output with all current sources on.

R55, R56, and R57 may be adjusted to correct for various offset voltages present in the system. By selecting these resistors, the ladder output can be varied to ±12.5 millivolts.

It is suggested that clamp diodes be added to the collectors of the 2N995 transistors. This will eliminate the necessity for tight control on the 2N995 collector current. If the current is too high, the reverse emitter-base breakdown (5v) of the 2N930 current source transistors will be exceeded feeding current into the base reference supply impairing the regulation.

If the current is too low, the 2N930 transistors will not be cut off. With clamp diodes, the voltage swing of the control flip-flops will not be critical and the 2N995 current can be set to meet the worst-case minimum requirements of 0.5 milliamperes without causing the 2N930 transistors to break down when the worst-case maximum current flows.

It is suggested that the T.I. SN522 comparator operational amplifier be replaced by a Fairchild μA709 amplifier, which has better specifications. This should make it easier to get good performance in production runs.

The most objectionable characteristic of the T.I. unit is its common mode rejection ratio of 50db (300:1). For a 6.4 volt input variation, this would cause an offset error of 21 millivolts (±10.5 mv). In contrast the μA709 common mode rejection ratio is 70db (3000:1) giving a ±1 millivolt error.

SECTION 4

ANALOG INPUT GATE SWITCH ANALYSIS

The Analog Input Gate switch shown in Figure 4-1 has a very low base drive of 18 microamperes. In addition, the series diodes are driven by SN510 flip-flops which provides questionable operation at temperature extremes because of voltage swing limitation. To ensure reliable operation, it is recommended that base drive of the gate switch be increased by lowering the 1-megohm resistor to 0.1 megohms and that the C2, C3, C4, and C5 flip-flops be changed to the SN511 type. The SN511 type has the sufficient drive and voltage swing to provide a solid turn-on or turn-off condition over the operating temperature range.

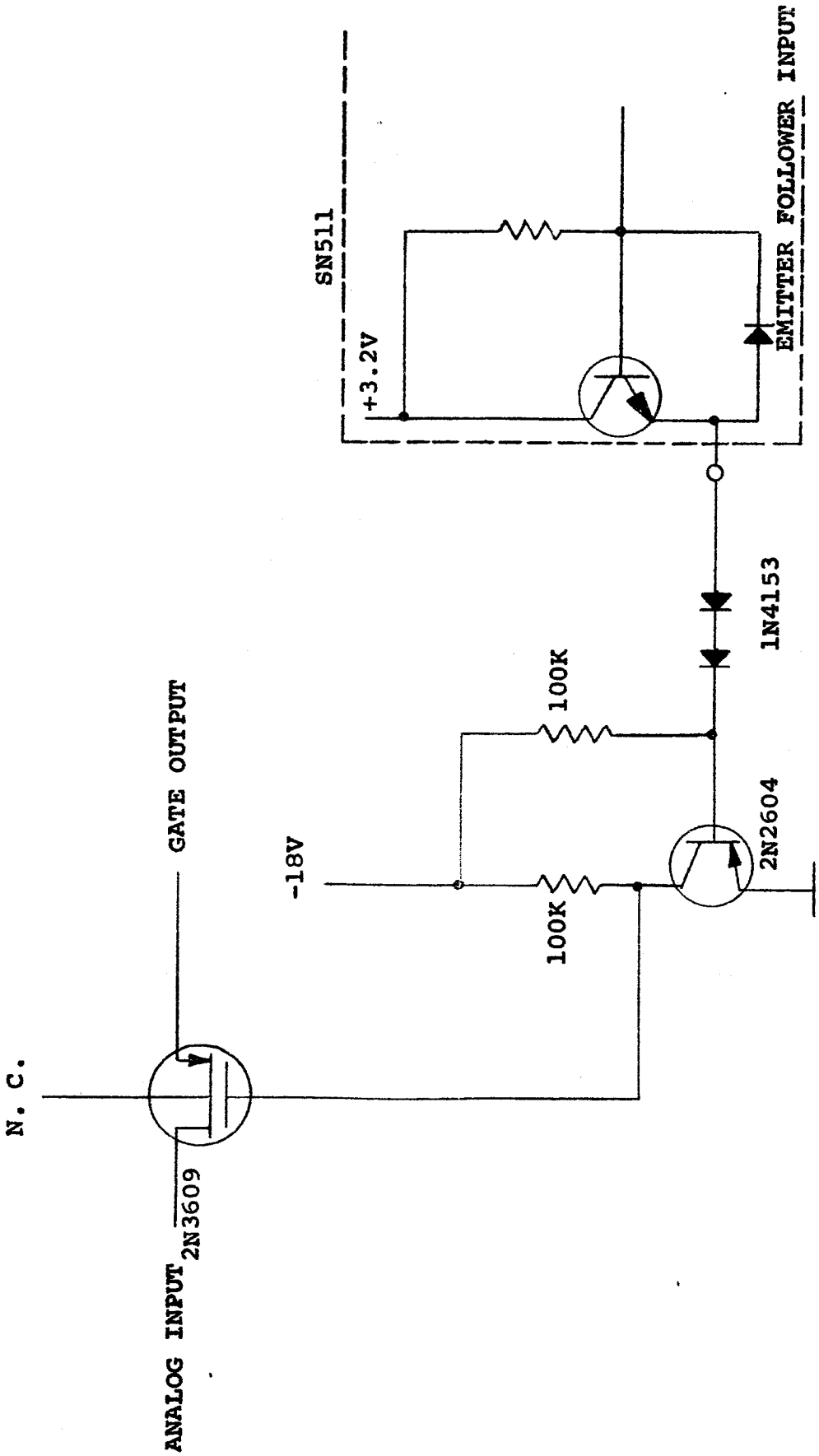


FIGURE 4-1

Analog Input Gate Switch

SECTION 5

LOGICAL DESIGN ANALYSIS

The evaluation of the logical design schematics MD2210 Ⓑ dated 26 October 1965, and MD2165 © dated 26 October 1965, was made. A detailed analysis was made on timing, loading, and possible race conditions. The only questionable timing problem, if it is a problem, is the asynchronous operation of the exclusive "OR" gate which is generating the diphase tape output signal. All signals are not appearing at the gate inputs simultaneously; therefore, the gate output can fluctuate because B1 or $\overline{B1}$ is occurring before the F flip-flop output. Figure 5-1 shows a typical case.

Other areas which are questionable because of logical mechanization concerns the Frame Sync logic gates and Frame Sync inhibit gates.

The Frame Sync format as generated by the logic does not agree with the format in drawing MB2215. The Frame Sync logic generates the pattern 00011101 while the Frame Sync format drawing shows the pattern to be 10111000. The Frame Sync logic generates a format which is 180° out of phase with the analog data conversion. To be compatible the Frame Sync gating should be as shown in Figure 5-2.

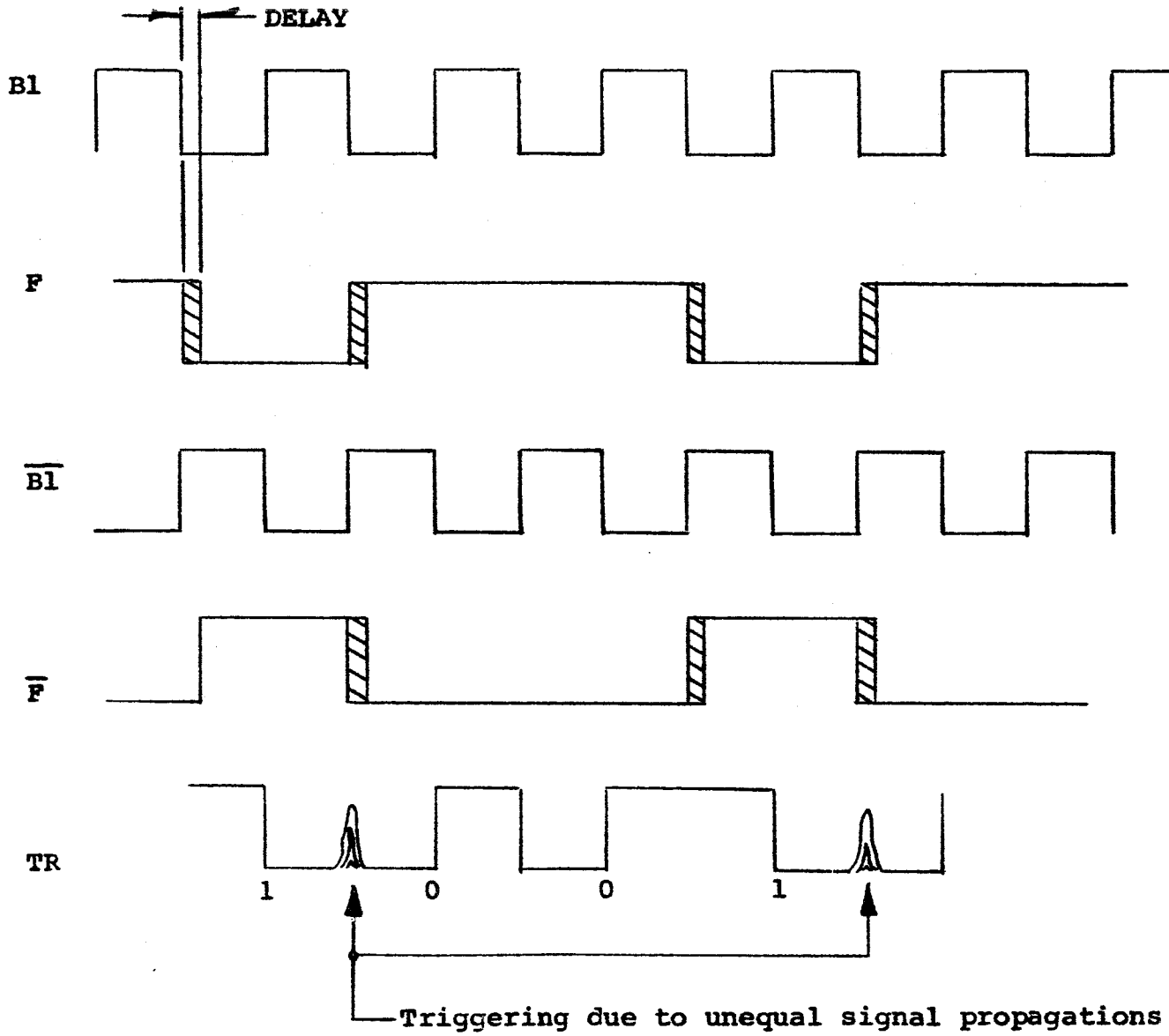


FIGURE 5-1

Tape Recorder Buffer Output

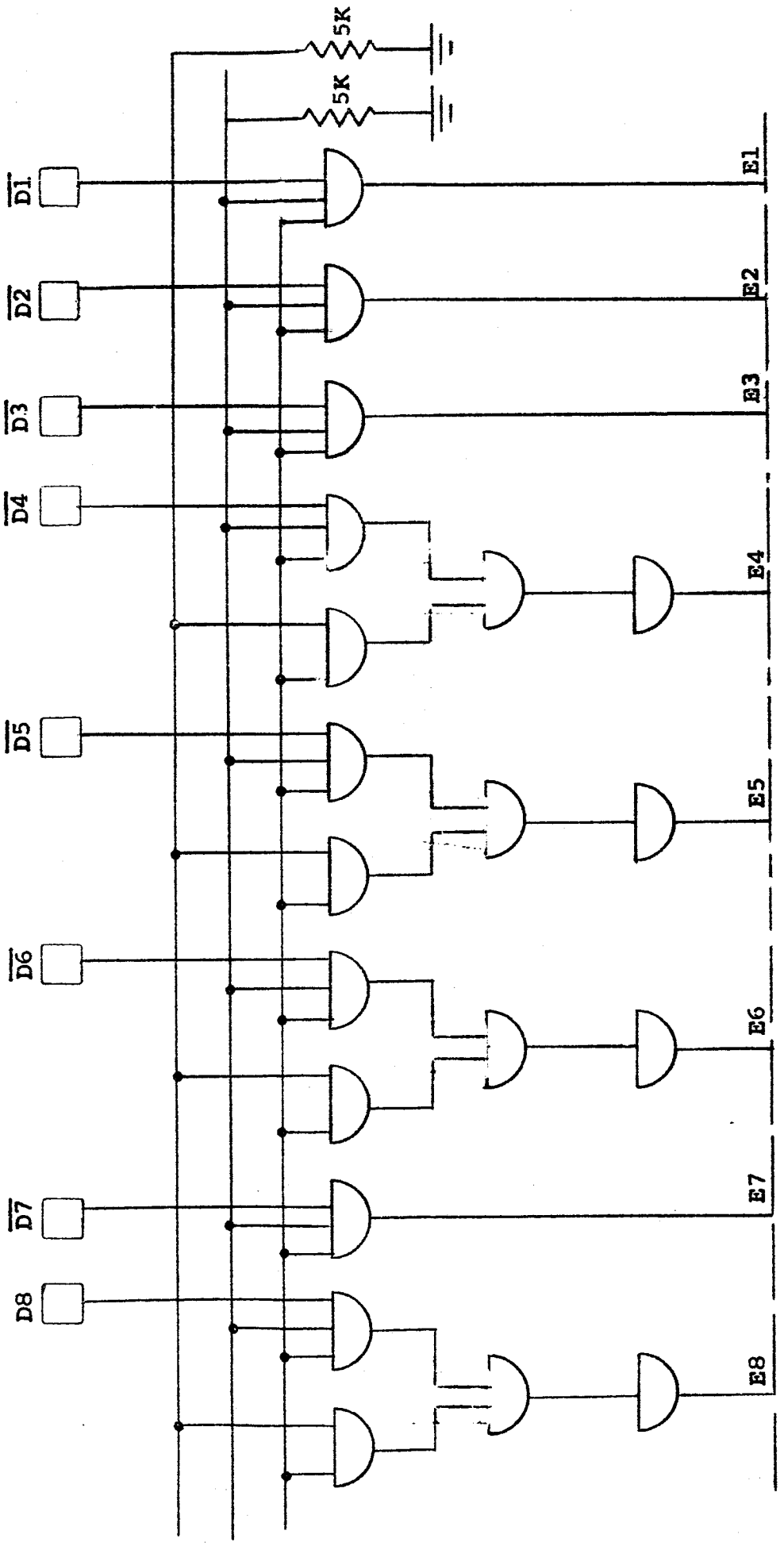


FIGURE 5-2

Frame Sync Gating

The Frame Sync Inhibit (FSI) logic does not include the $\overline{D2}$ term. The exclusion of this term indicates that two conditions of error can exist. The FSI logic will change the least-significant-bit (LSB) to a one if the logical configuration of the D flip-flops is 10111010 or 10111000. An extender gate is required to pick up the $\overline{D2}$ term so that the LSB will be changed only when the Frame Sync word appears. The logic change is shown in Figure 5-3.

5.1 BENCH TEST SYNCHRONIZATION

The B1 flip-flop which provides the 1.66K signal is a SN510 flip-flop. It has a fan-out limitation of four and is required by the bench tester for synchronization. The fan-out of this flip-flop exceeds the manufacturer's recommendations if the BTE is tied in. To alleviate the problem, it is suggested that the B1 flip-flop be changed to a SN511 type which has increased fan-out capability.

5.2 INTEGRATED CIRCUIT LOGIC MECHANIZATION

In several cases, there is a logical representation as shown in Figure 5-4A. The logic calls out for this representation, the use of a SN514 network which is interconnected as shown in Figure 5-4B. The mechanization requires eight interconnections -- three logic inputs, three ground points, and two outputs. The use of a SN515 as shown in Figure 5-4C can be mechanized to perform the same function except that the number of interconnections is reduced to four: two logic inputs, one logic output, and two ground points. The reduction in interconnections means less printed circuit lines and higher reliability. CalComp recommends that this logical mechanization be used wherever possible.

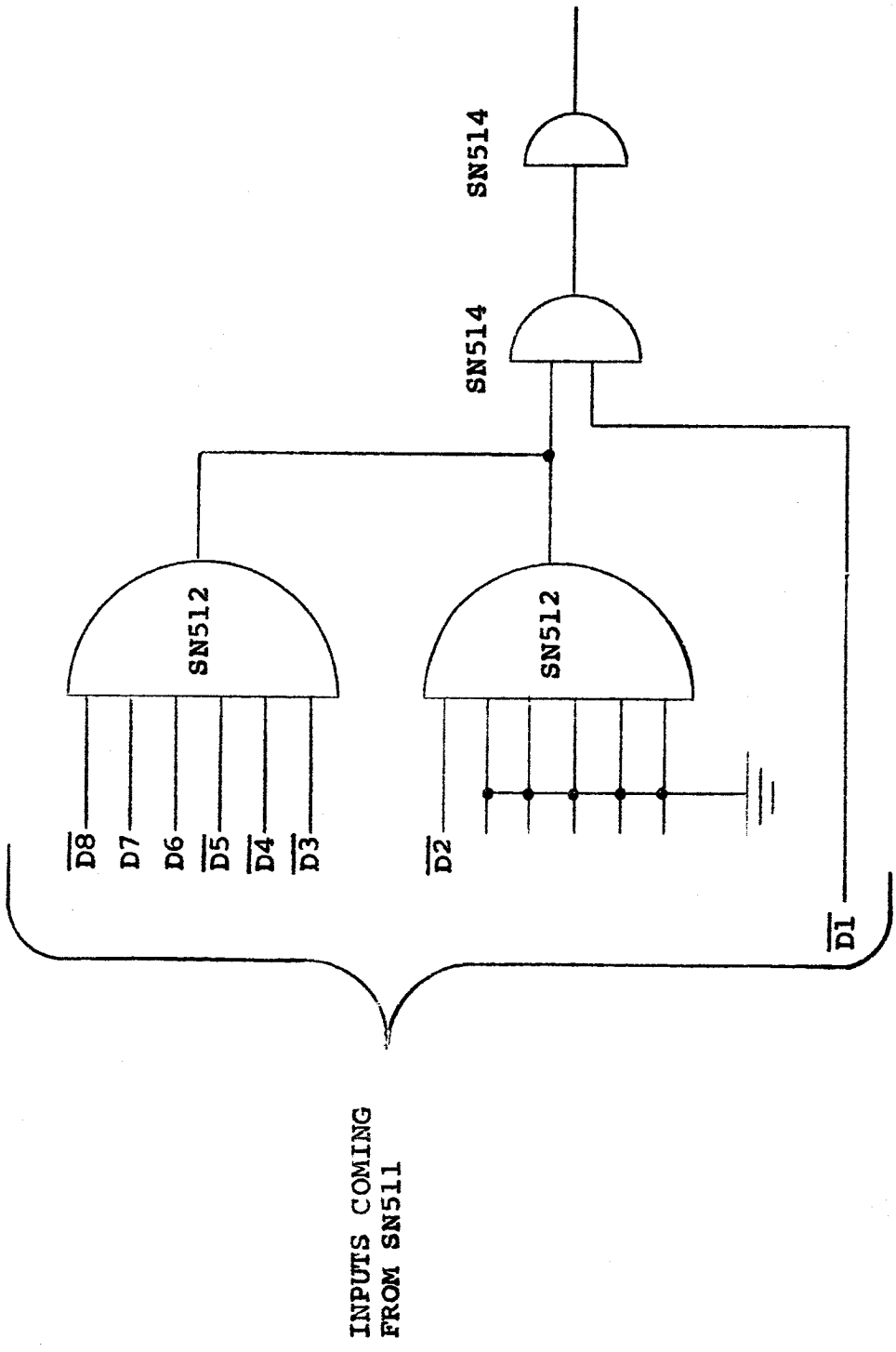
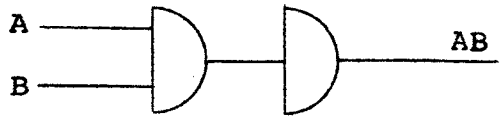


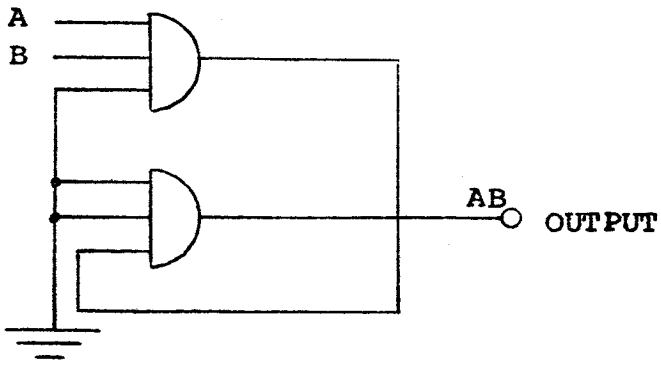
FIGURE 5-3
Frame Sync Inhibit Logic



LOGICAL REPRESENTATION

Interconnection using SN514

(A)

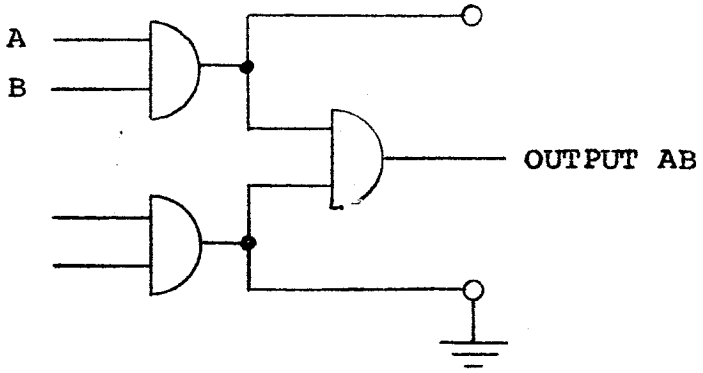


REQUIRES:

1. Three logic inputs.
2. Three grounding points
3. Two outputs.

Eight interconnections

(B)



REQUIRES:

1. Two logic inputs.
2. One logic output.
3. One grounding point.

Four interconnections.

(C)

FIGURE 5-4

Logical Mechanization

SECTION 6

DEVELOPMENT STUDY REQUIREMENTS

The developmental aspect of the MRIR Telemetry Unit includes the following areas:

a. Circuit Design

b. Mechanical Design

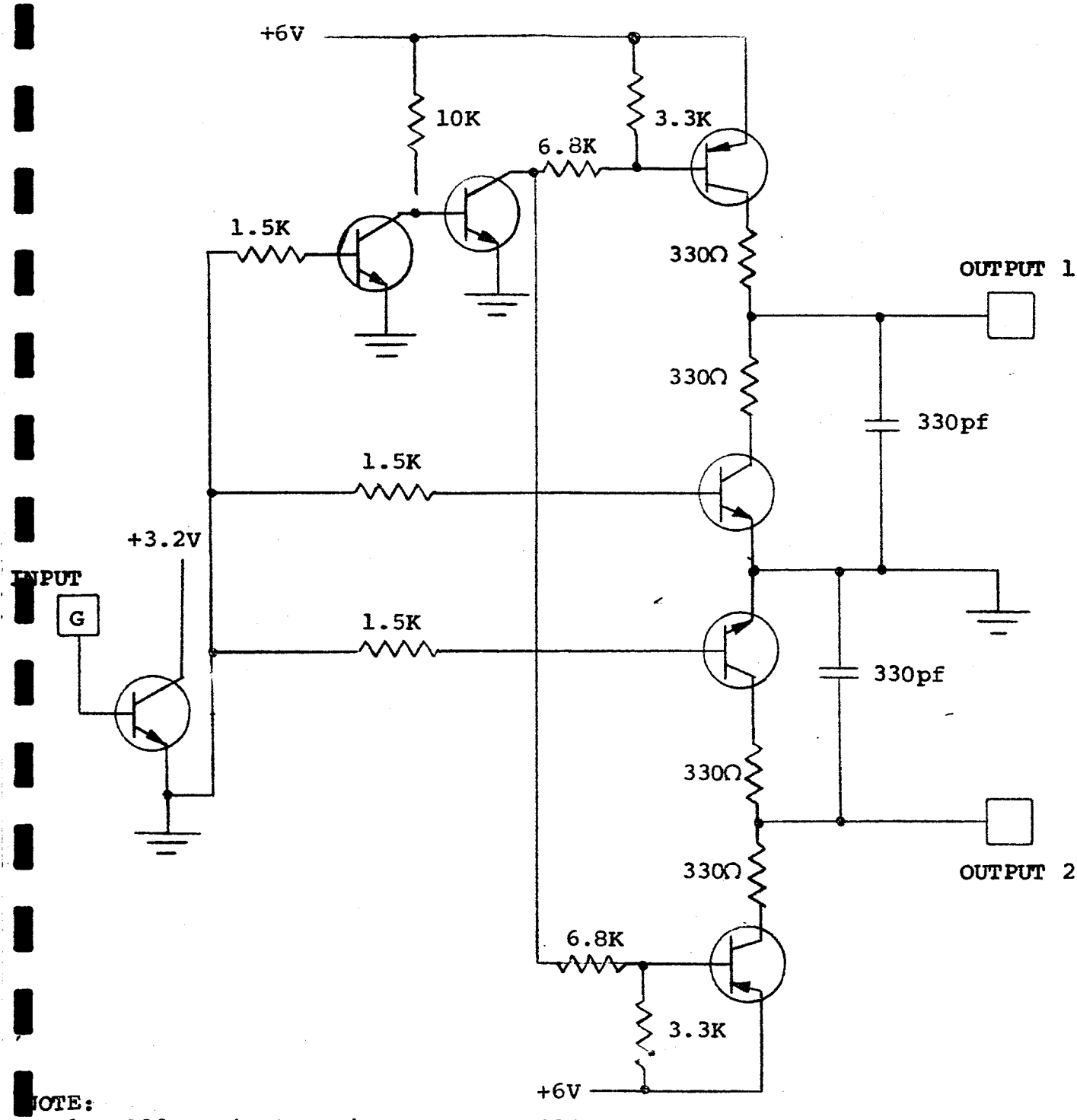
c. Interface Specification

d. Test Procedures

6.1 CIRCUIT DESIGN

6.1.1 BUFFER OUTPUT

The circuit design for the MRIR consisted of developing a buffer output from the MRIR data output register to the tape recorder unit. The circuit design specifications were listed in the memorandum from John Lesko to Harold Zaret, dated 8 November 1965, paragraph 1.2. The schematic for the buffer output is shown in Figure 6-1. In this circuit, a push-pull output is used for data transmittal. The circuit utilizes an emitter-follower buffer stage (Q1) because of the low fan-out capability of the SN515 network. Transistors Q2 and Q3 serve as intermediate switches to provide positive turn-on and turn-off control and Q4 and Q5 are the push-pull output drivers for Buffer No. 1 and Q6 and Q7 are the push-pull output drivers for Buffer No. 2.



NOTE:
1. All NPN's transistors are 2N2369.
2. All PNP's transistors are 2N995.

FIGURE 6-1

Tape Recorder Output Buffer Circuit

The buffer output amplifiers are inverters with respect to Point G. Point G, according to the Frame format drawing, is 180^{o} out of phase; however, the buffer output brings it back into agreement. The power dissipation for one buffer output driver is approximately 15 milliwatts at a 50-percent duty cycle with the tape recorder equivalent circuit as the output load. The output impedance is 330 ohms and the circuit provides short circuit protection.

The circuit operation is as follows: The input to the emitter-follower swings between 0 volts and +3.2 volts nominally. With the input at ground, Q2 is off, Q3 is on and the voltage divider between 3.3K and 6.8K to +6 volts turns Q4 on. Q5 is held off. With the input at +3.2 volts, Q2 is turned on, Q3 and Q4 are turned off, and Q5 is turned on, which provides a ground output through 330 ohms.

6.1.2 TELEMETRY POINTS

Three telemetry points are required to monitor the MRIR Telemetry Unit. The telemetry points indicate the state of the ON-OFF power relay, the -12 volt power supply and the hottest point in the MRIR Telemetry Unit. Since telemetry points can utilize either analog or digital channels, the allocation of the telemetry points for the MRIR is that the relay use the digital channel and the -12 volts and temperature use the analog channels.

All telemetry point outputs are derived by simple divider networks in conjunction with the NIMBUS Handbook for Experimenters (NIMBUS "B"). The networks including nominal output voltage and output impedance is shown in Figure 6-2.

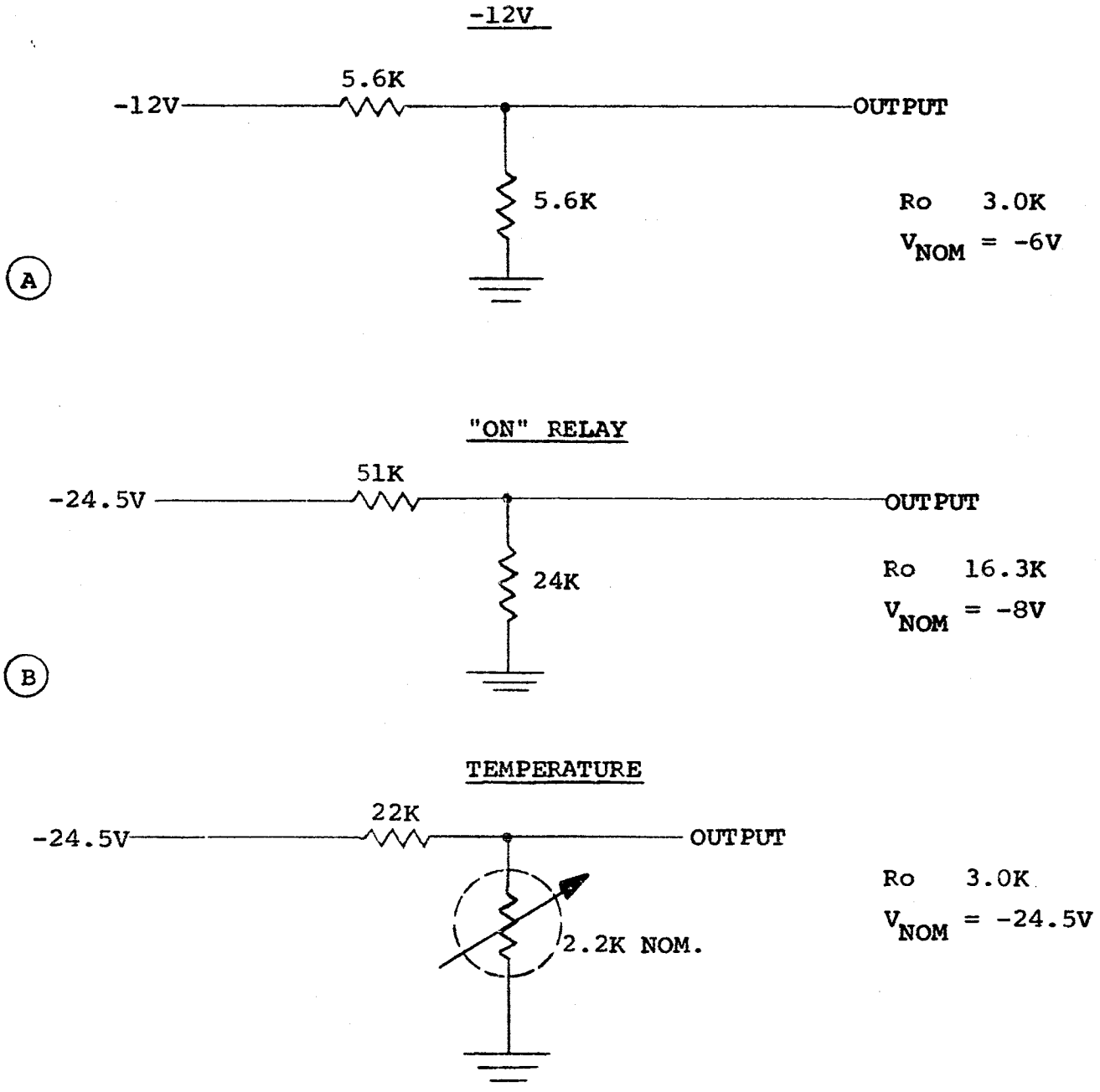


FIGURE 6-2

Telemetry Points

6.2 MECHANICAL DESIGN

The mechanical design includes the areas of packaging, printed circuit boards, thermal, weight, and stress analysis.

6.2.1 PACKAGING

The packaging of the MRIR Telemetry Unit conforms to the requirements specified in the GSFC specification for NIMBUS "B." The housing which includes the covers will be of magnesium and finished with a DOW 17, Type 1, Class C protective coating. The housing size is 6 x 4 x 6.5 inches. This size meets the standard module size of 2 over 0. A set of detailed mechanical design drawings can be found in Appendix A.

The housing will contain five interface connectors of the Cannon Series D type. A more exact description of these connectors including interface specifications will be contained in Section 6-3 of this report.

6.2.2 PRINTED CIRCUIT BOARDS

The housing is designed to contain seven printed circuit boards of the type shown in the outline drawing in Figure 6-3. The board has a metal plate across the top which provides a heat path from the printed circuit components, through the metal plate to the chassis. The metal plates serve to add rigidity and are used to clamp the printed circuit board to the chassis by screws. The bottom of the printed circuit board requires a 44-pin printed circuit connector.

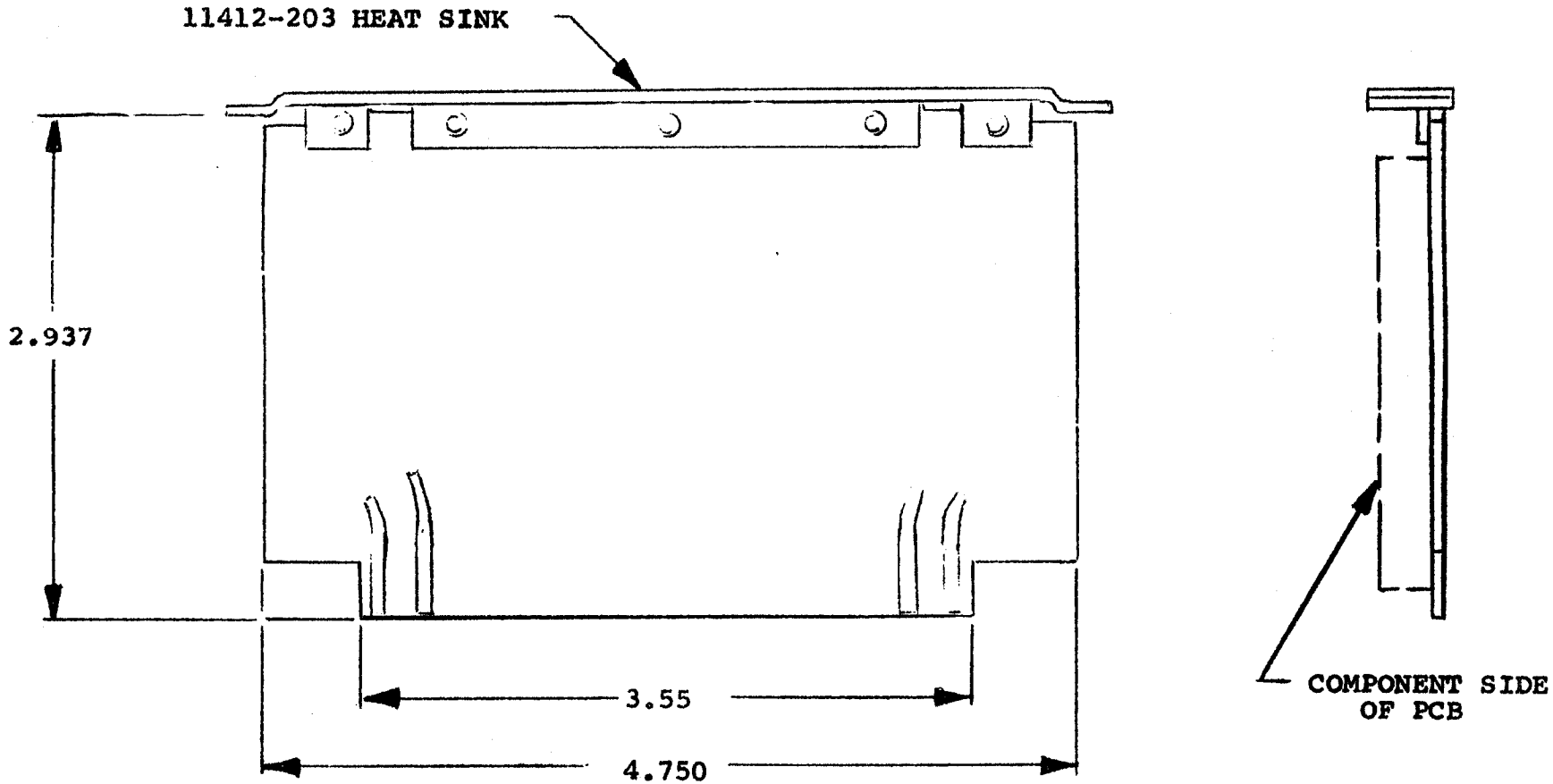


FIGURE 6-3

Printed Circuit Board Outline Drawing

The seven printed circuit boards required are as follows:

a. Power Supply No. 1

b. Power Supply No. 2

c. Frame Sync and Data Output

d. Encode Generator - Timing Generator

e. Analog Input - 25-kc Generator

f. A/D Converter

g. A/D Control

The allocation of these printed circuit boards within the MRIR Telemetry Unit chassis is shown in Figure 6-4. Shielding is provided to attenuate any spikes which may be generated by the flux oscillator supply. The placement of the analog input module is to isolate it from the DC/DC Converter as well as other changing signals being generated, and also to keep its input lines as short as possible. Further, a ground rule for interconnection wiring will be to keep away from the analog input lines, any signal which is capable of producing crosstalk.

6.2.2.1 Material List

Presented in Table 6-1 is a material list of all the components to be used in the MRIR Telemetry Unit. The material list contains information on type of component, value rating, manufacturer and manufacturer's type designation; maximum electrical stress levels experienced during the subsystem operation is listed separately. Table 6-2 lists the T.I. integrated networks used.

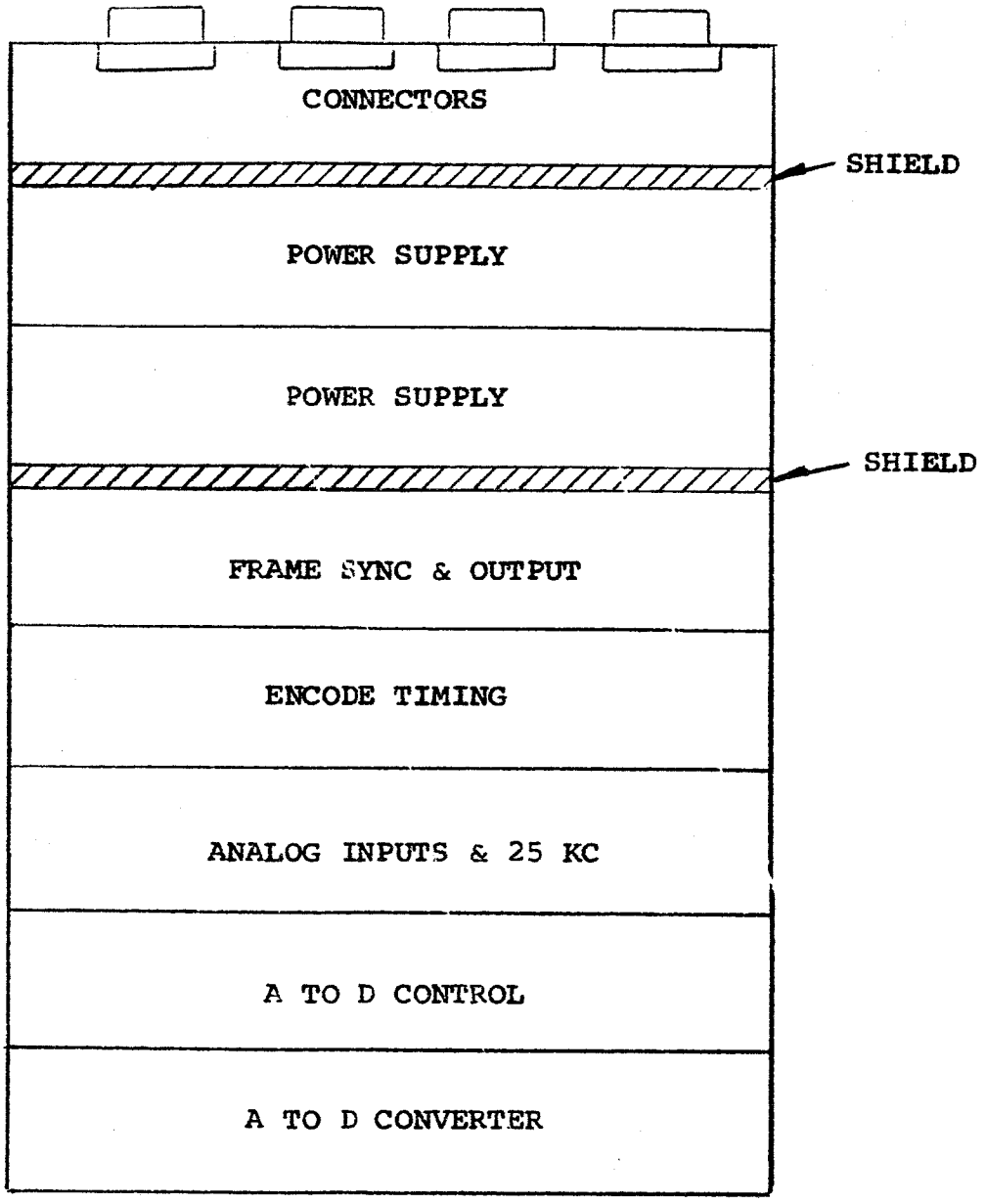


FIGURE 6-4

Printed Circuit Board Layout

In some cases, the parts chosen are deviations from the parts specified on the drawings; however, the parts chosen as deviations are of equivalent or superior value. For instance, Kemet capacitors are called out over 150D Sprague's because the Kemet capacitors will be 100 percent screened and noise tested and delivered in adequate time for the schedule to be met. Furthermore, Kemet capacitors were used on the NIMBUS "C" MRIR-PCM development.

TABLE 6-1

MRIR-PCM Electro-mechanical Parts List

Type	Value	Manufacturer	Manufacturer Type
Connector	9-pin male	Cannon	DEM-9P-NMB-2
Connector	9-pin female	Cannon	DEM-9S-NMB-2
Connector	15-pin male	Cannon	DEM-15P-NMB-2
Connector	15-pin female	Cannon	DEM-15S-NMB-2
Connector	37-pin female	Cannon	DEM-37S-NMB-2
Connector	44-pin printed circuit	Masterite	BR22DRXI
Transformer (P.S.)		Magnetic, Inc.	No. 52168-1F
Resistor	4.7Ω ± 2%	Corning	C07 4.7
	51Ω ± 2%		C07 51
	330Ω ± 2%		C07 33
	470Ω ± 2%		
	820Ω ± 2%		
	1.0K ± 2%		
	1.2K ± 2%		
	1.5K ± 2%		
	3.3K ± 2%		
	4.7K ± 2%		
	5.1K ± 2%		
	5.6K ± 2%		
	6.8K ± 2%		
	8.2K ± 2%		
Resistor	10.0K ± 2%	Corning	C07 33

Type	Value		Manufacturer	Manufacturer Type
Resistor	15.0K ± 2%		Corning	C07 33
	22.0K ± 2%		Corning	C07 33
	24.0K ± 2%		Corning	C07 33
	27.0K ± 2%		Corning	C07 27K
	68.0K ± 2%		Corning	C07 68K
	100K ± 2%		Corning	C07 100K
	200K ± 2%		Corning	C07 200K
	12.0K ± 2%	1/8 W, T.C. of 2 ppm	Kelvin	
	20.0K ± .05%		Kelvin	
	15.0K ± .05%		Kelvin	
	10.0K ± .05%		Kelvin	
	392 Ω ± 1%		I.R.C.	RN60B/D
	499 Ω ± 1%			
	909 Ω ± 1%			
	1.43K ± 1%			
	1.47K ± 1%			
	1.5K ± 1%			
	1.54K ± 1%			
	1.58K ± 1%			
	5.36K ± 1%			
	5.49K ± 1%			
	5.62K ± 1%			
	5.76K ± 1%			
	5.9K ± 1%			
	6.65K ± 1%			
	9.09K ± 1%			
	9.31K ± 1%			
	9.53K ± 1%			
Resistor	9.76K ± 1%		I.R.C.	RN60B/D

Type	Value	Manufacturer	Manufacturer Type
Resistor	10K ± 1%	I.R.C.	RN60B/D
Resistor	46.4K ± 1%	I.R.C.	RN60B/D
Resistor	56.2K ± 1%	I.R.C.	RN60B/D
Resistor	61.9K ± 1%	I.R.C.	RN60B/D
Transistor	2N2658	Honeywell	
	2N1132B	Fairchild	
	2N2927	Sylvania	
	2N930	Fairchild	
	2N995	Fairchild	
	2N2369	Fairchild	
	2N2604	T.I.	
Transistor	2N3609 (F.E.T.)	G.M.E.	
Diode	1N3730	Raytheon	
Diode	1N4153	GE	
Zener	1N748A	Motorola	
Zener	1N753A	Motorola	
Zener	1N759A	Motorola	
Zener	1N457A	Motorola	
Inductance	10 μh	J. W. Miller	9320-30
Transformer (200 kc)	CORE	Magnetic, Inc.	52168-1F
Relay	Mag. Latching	Potter & Brumfield	SL11DB
Operational Ampl.	μA709	Fairchild	

Type	Value	Manufacturer	Manufacturer Type
Capacitor	0.022µfd ± 10% 50vdc	Kemet	KGR022J50 KMS
	0.047µfd ± 10% 50vdc		KGR047J50 KMS
	0.10 µfd ± 10% 50vdc		
	2.2 µfd ± 10% 50vdc		KG2R2 J50 KMS
	2.2 µfd ± 10% 20vdc		KG2R2 J20 KMS
	3.3 µfd ± 10% 15vdc		KG3R3 J15 KMS
	6.8 µfd ± 10% 6vdc		KG6R8 J6 KMS
	6.8 µfd ± 10% 35vdc		KG6R8 J35 KMS
	10.0 µfd ± 10% 20vdc		KG10 J20 KMS
	15.0 µfd ± 10% 20vdc		KG15 J20 KMS
	22.0 µfd ± 10% 15vdc		KG22 J15 KMS
	22.0 µfd ± 10% 35vdc		KG22 J35 KMS
	22.0 µfd ± 10% 50vdc		KG22 J50 KMS
	82.0 µfd ± 10% 20vdc		KG82 J20 KMS
	220.0µfd ± 10% 10vdc		KG220 J10 KMS
	270.0µfd ± 10% 6vdc	Kemet	KG270 J6 KMS
	47.0 pfd ± 10% 500vdc	Corning	CM15 C 470 J
	68.0 pfd ± 10% 500vdc		CM10 C 680 J
	100.0pfd ± 10% 500vdc		CM15 C 101 J
	220.0pfd ± 10% 500vdc		CM15 C 221 J
	330.0pfd ± 10% 500vdc		CM15 C 331 J
	470.0pfd ± 10% 500vdc		CM15 C 471 J
Capacitor	680.0pfd ± 10% 500vdc	Corning	CM15 C 681 J

TABLE 6-2

Total TI IC's Used

1. Frame Sync and Data Input Module

SN 510	9
SN 514	6
SN 515	5

2. Analog Input and 25-kc Generator

SN 510	3
SN 511	5
SN 512	1
SN 514	1
SN 515	1
SN 517	2

3. Analog-to-Digital Data Control Logic

SN 510	8
SN 511	8
SN 512	2
SN 514	1
SN 515	8

4. Timing Generator

SN 510	8
SN 511	1
SN 512	1
SN 513	2
SN 514	2
SN 515	1
SN 517	3

5. DC to DC Converter

SN 521	1

6.2.2.1.1 Component Electrical Stress Analysis

An analysis has been made of the electronic components in the system to determine if any critical electrical stresses were being applied. Outside of the analysis on the Q6 and Q7 rectifier transistors used in the DC/DC Converter and the input filter capacitor of 35 volts dc, no other critical areas have been found.

The ladder resistors are rated at 1/8 watts. The power dissipation of these resistors is considerably less than 60 milliwatts. All 1/4 watt resistors are below 125 milliwatts. All capacitors have their rated working d-c voltages at close to two times or better than the levels actually being used. One exception is using a 6-volt capacitor for the +3.2 volt supply. Transistors, diodes, and Zener diodes are being utilized well within manufacturer's recommendations. The Zener diodes, in particular, are being used at their test current rating. Since the MRIR requires low power for operation, no input/output connector pin, including the pins to route power to the Radiometer subsystem, are near their rated 5 amp per pin capacity. Milliampere currents are applied to the printed circuit board connectors. All IC's are operating within manufacturer's operating recommendations.

6.2.3 THERMAL ANALYSIS CONDITIONS AND ASSUMPTIONS

The heat produced by the power dissipation is transferred from the MRIR-PCM Telemetry Unit to the spacecraft structure. To determine the heat flow and the temperature drops, the following conditions were used.

a. The transfer of heat is considered to be entirely by conduction. Convection cannot occur because the unit operates in a vacuum, and the heat transferred by radiation is so slight that it is being neglected.

b. The thermal conductivity of the magnesium chassis (ZK60A) is 2980 milliwatts/in.^{2} ^{o}C/in.

c. The thermal conductivity of the aluminum brackets on the printed circuit boards is 3940 milliwatts /in.^{2} ^{o}C/in.

d. The copper clad on the printed circuit boards has a thermal conductivity of 9850 milliwatts/in.^{2} ^{o}C/in.

e. Experimentally a joint of two DOW No. 17 coated parts proved to have a thermal conductivity of 500 milliwatts/in.^{2} ^{o}C. A joint made of a DOW No. 17 coated part and a base metal part has a thermal conductivity of 250 milliwatts/in.^{2} ^{o}C.

f. The printed circuit board, Type GE, has a thermal conductivity of 5.1 milliwatts/in.^{2} ^{o}C/in.

g. The polyurethane coating on the assembled printed circuit boards has a thermal conductivity of 28.9 milliwatts/in.^{2} ^{o}C/in.

6.2.3.1 Temperature Differential Between Components and Sparecraft Structure

The assumed heat path of the power dissipated on the printed circuit boards is through the printed circuit board mounting brackets into the chassis walls, out the top plate, and into

the spacecraft structure. Under this assumption the calculations for the temperature drop is divided into two parts. First, the individual printed circuit board temperature drops from the components to the chassis; second, the temperature drop caused by the total power dissipated from the chassis to the spacecraft structure.

a. Temperature drop from individual printed circuit to chassis.

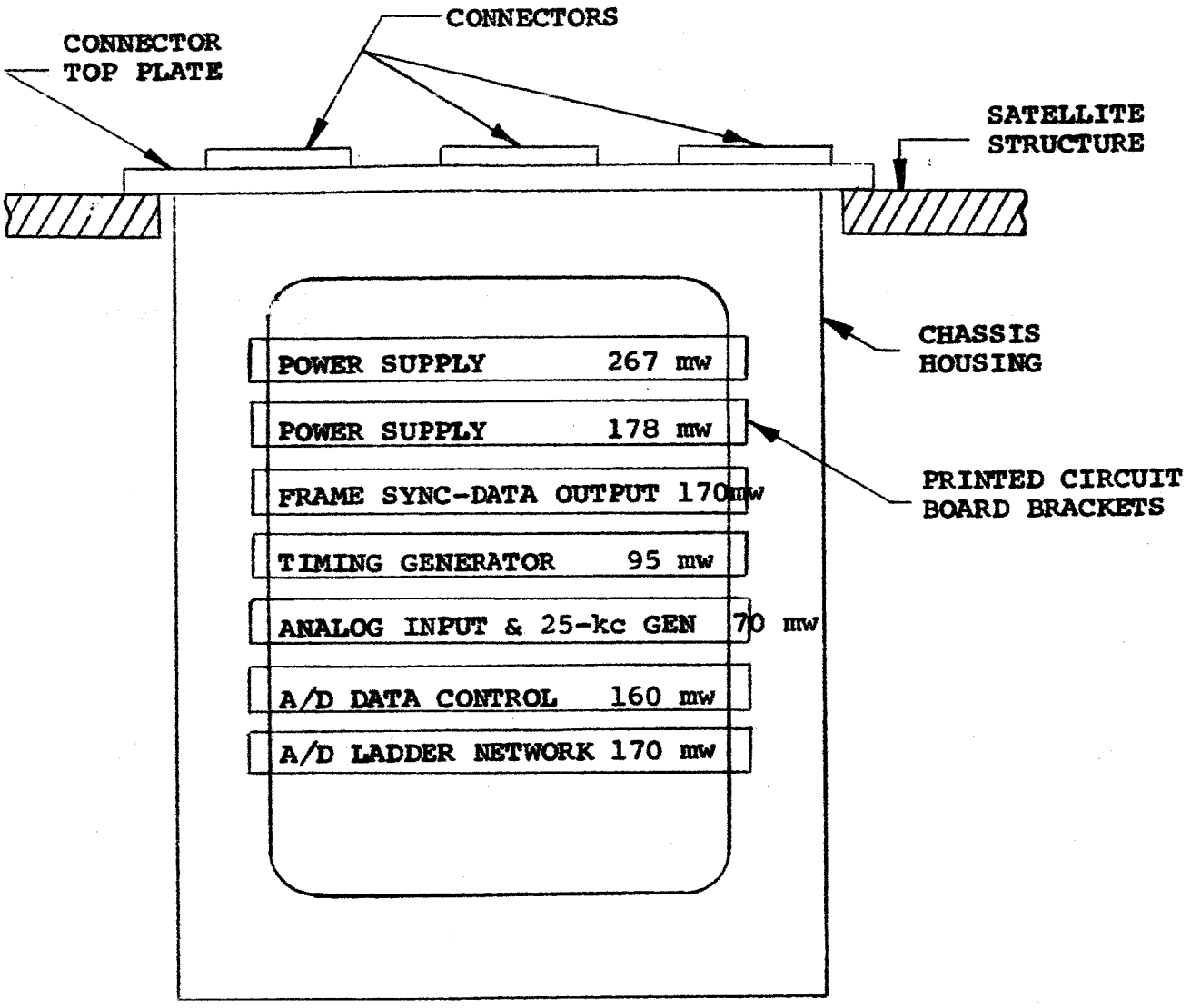
The power dissipated by each printed circuit board is shown on Figure 6-5 along with the boards location inside the chassis. Figure 6-6 shows a typical printed circuit board.

(1) A/D Data Control

As shown on Figure 6-5, this printed circuit board has a heat dissipation of 160 milliwatts. The temperature drop from the surface of the printed circuit board to the chassis is broken down into three steps.

(a) surface of printed circuit board to bracket (on Figure 6-6, 1 to 2)

$$T = \frac{\text{heat dissipated x distance of heat flow}}{\text{thermal conductivity x area perpendicular to flow}}$$



Total power dissipated is 1.10 watts

FIGURE 6-5

Power Dissipation Breakdown

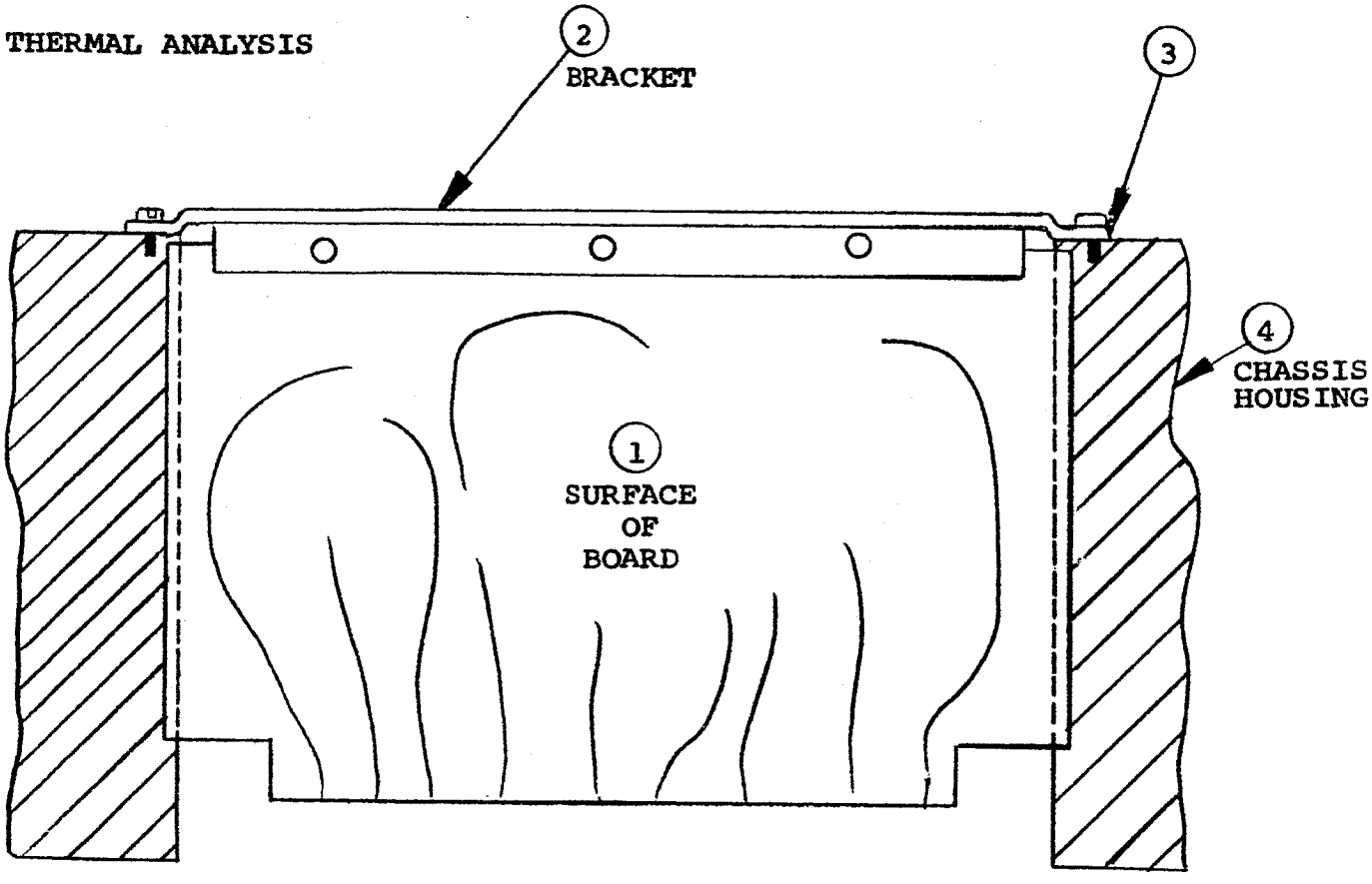


FIGURE 6-6

PCB Thermal Analysis Considerations

$$T = \frac{160 \text{ milliwatts} \times .125 \text{ in.}}{5.1 \text{ mw/in.}^2 \ ^{o}\text{C/in.} \times 4.125 \text{ in.} \times .059 \text{ in.}}$$

$$T = 16.15 \ ^{o}\text{C}$$

(b) The temperature drop through the aluminum bracket (Figure 6-6, 2 to 3).

$$T = \frac{160 \text{ mw} \times 1.0 \text{ in.}}{3940 \text{ mw/in.}^2 \ ^{o}\text{C/in.} \times .042 \text{ in.}^2} + \frac{160 \text{ mw} \times .43 \text{ in.}}{3940 \text{ mw/in.}^2 \ ^{o}\text{C/in.} \times .027 \text{ in.}^2}$$

$$T - 1.59 \ ^{o}\text{C}$$

(c) The temperature drop across the joint between the base aluminum bracket and the magnesium chassis coated with DOW No. 17.

$$T = \frac{160 \text{ mw}}{250 \text{ mw/in.}^2 \ ^{o}\text{C} \times .250 \text{ in.} \times .437 \text{ in.}}$$

$$T - 5.85 \ ^{o}\text{C}$$

(d) The total temperature drop from the surface of the printed circuit board to the chassis is 23.6 ^{o}C.

(2) A/D Ladder Network

This printed circuit board dissipates 170 milliwatts which causes a temperature drop of 25 °C from the printed circuit board to the chassis. An aluminum strap connects the five double transistors thermally together assuring that there is no temperature difference between them.

(3) Analog Input and 25-kc Generator

This printed circuit board dissipates 70 milliwatts, giving a temperature drop to the chassis of 10.21 °C.

(4) Timing Generator

The heat dissipation is 95 milliwatts which causes a temperature drop of 14.0 °C from the printed circuit board to the chassis.

(5) Frame Sync - Data Output

The heat dissipation is 170 milliwatts, giving a temperature drop of 25 °C.

(6) Power Supply

The power supply is divided into two printed circuit boards dissipating 268 and 178 milliwatts. The temperature drop is 30 °C and 21 °C, respectively.

b. Temperature Drop from Chassis to Spacecraft Structure

The power dissipated by the individual printed circuit boards totals 1.11 watts. This total power dissipation can be used to determine the temperature drop from the chassis to the spacecraft structure. The heat flow between these two parts go through four series conductors.

(1) The heat dissipated from the printed circuit boards is quite evenly balanced about the center printed circuit board. To simplify calculation, the total heat flow in the magnesium chassis sides will be considered to originate from the mounting surface of the middle printed circuit board (Timing Generator) and flow to the chassis surface adjoining the top plate. Since the mounting surface is on the edge of the chassis sides, the effective area for heat flow is assumed to be about half the side area.

$$T = \frac{\text{heat dissipation x distance of heat flow}}{\text{thermal conductivity x area perpendicular to flow}}$$

$$T = \frac{1110 \text{ mw} \times 3.75 \text{ in.}}{2980 \text{ mw/in.}^2 \ ^\circ\text{C/in.} \times 1.32 \text{ in.}^2}$$

$$T = 1.06 \ ^\circ\text{C}$$

(2) The temperature drop due to the DOW No. 17 coating on the chassis and top plate.

$$T = \frac{1110 \text{ milliwatts}}{500 \text{ mw/in.}^2 \ ^\circ\text{C} \times 5.15 \text{ in.}^2}$$

$$T = 0.43 \ ^\circ\text{C}$$

(3) The temperature drop in the top plate (magnesium).

$$T = \frac{1110 \text{ mw} \times 0.59 \text{ in.}}{2980 \text{ mw/in.}^2 \text{ }^{\circ}\text{C/in.} \times 1.3 \text{ in.}^2}$$

$$T = 0.18 \text{ }^{\circ}\text{C}$$

(4) The temperature drop due to the DOW No. 17 coating on the top plate and the spacecraft structure.

$$T = \frac{1110 \text{ mw}}{500 \text{ mw/in.}^2 \text{ }^{\circ}\text{C} \times 3.0 \text{ in.}^2}$$

$$T - 0.73 \text{ }^{\circ}\text{C}$$

(5) The total temperature drop between the chassis walls and the spacecraft structure is 2.4 $^{\circ}$C.

6.2.3.2 Conclusions

The thermal analysis points out that the hottest components will be on the first power supply board. The primary power pre-regulator transistor is the true hot spot. Since this transistor can give off approximately 160 milliwatts of power dissipation, a heat path to the printed circuit board bracket will be used to keep the temperature not higher than 30 $^{\circ}$C above ambient.

6.2.4 WEIGHT ANALYSIS

A comprehensive study has been made to determine the weight of the MRIR Telemetry Unit. In instances where material of the type to be used in the telemetry unit was on hand, actual measurements were made. An example is the DC/DC Converter breadboard. Corrections were made to allow for the phenolic board and mounting brackets. The weight analysis is contained in Table 6-3.

TABLE 6-3

MRIR Weight Breakdown

Total Weight

Cover (Bracket Side)		.190 lbs
Cover (Connector Side)		.190
Top Plate		.205
Chassis		1.400
Connector (Cannon) (5)	46.3 grams	
Connector Plate		.051
A/D Data Control	54.55	
A/D Ladder	72.45	
Analog	65.65	
Timing	54.05	
Frame	60.15	
Power Supply 1	118.15	
Power Supply 2	211.95	
Wire	34.5	
Screws	40.0	
Connector Potting	60.0	
	817.75 grams =	1.80 lbs.
		3.836 lbs.
Power Supply Shields (2) (Aluminum Boards)		.264
	Solder Ect.	4.100 lbs.
Solder, etc.		.050 lbs.
	TOTAL	4.150 lbs.

6.2.5 STRESS ANALYSIS

The static stress analysis assured the structural stability of the MRIR-PCM Telemetry Unit to withstand the environment that the NIMBUS "B" will encounter. The areas mainly considered were the areas affected by the following forces: (1) the force developed by the 30g acceleration and (2) the internal pressure when the package is suddenly put into a vacuum.

The weights shown on Table 6-3 were used to determine the stress caused by the 30g acceleration on the different parts and fasteners. These stresses with the safety factors are on Table 6-4.

The stress caused by the pressure inside the package were calculated two different ways. First, the package was assumed to be air tight. The pressure inside the package under this assumption is 14.7 psi above the external pressure. (This is an extreme condition.) The main parts affected are the two covers and the middle section of the top plate. The last three items on Table 6-4 show the results.

TABLE 6-4

Stress Analysis

Part Name & Number	Force or Pressure	Type of Stress	Stress	Safety Factor
Connector (Top) Plate No. 11411-203	118 lbs (30g)	Shear Against Structure	79 psi	240
Housing (Chassis) No. 11413-203	112 lbs (30g)	Tensile Stress in walls	53 psi	583
P.C.Board (Power Supply)	14 lbs Concentrate (30g)	Flexure	6,500 psi	9.7
Screws No. 6-32 Conn. Plate	118 lbs (30g)	Tensile	1,310 psi	22.9
Screws No. 4-40 Cover	5.7 lbs (30g)	Shear	119 psi	252
Screws No. 4-40 P.C. Board	14 lbs (30g)	Shear	584 psi	51.4
Connector (Top) Plate No. 11411-203	14.7 psi (Air Tight)	Tensile	6,930 psi	3.18
Cover * No. 11415-203	14.7 psi (Air Tight)	Tensile	14,850 psi	1.5
Screws No. 4-40 On Cover	14.7 psi (Air Tight)	Tensile	9,330 psi	7.5

*See Paragraph 6.2.5.

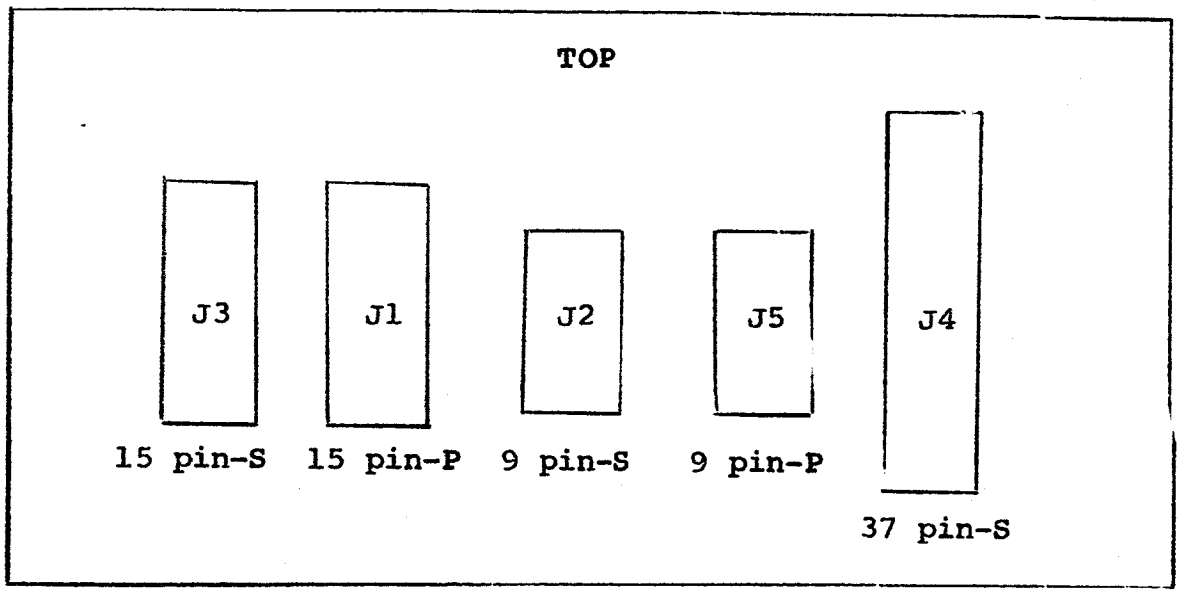
The other possible condition dealing with the pressure inside the package is that air can leak out around the connectors and through metal to metal points. When air can leak out, the covers are considered to be supported and not secured to the chassis frame as in the air tight condition. Under these conditions an air gap of .005 in.^{2} (.001 in. gap x 5 in. long) is needed to keep the safety factor higher than two. It must be pointed out that the air gap is a very conservative figure since the connector mountings are not sealed.

6.3 INTERFACE SPECIFICATION

The MRIR Telemetry Unit uses five input/output connectors. The connectors are Cannon gold-plated, Series D type which are arranged as shown in Figure 6-7. Table 6-5 indicates the type and function of each connector used. The connector and pin assignments have been made in accordance with the requirements of the MRIR NIMBUS "B" Telemetry GSFC specification and the NIMBUS Handbook for Experimenters (NIMBUS "B") dated October 1965. A deviation on one connector is undertaken because inputs and outputs are required on the same connector. Since the -24.5 volt primary power source is an output, this connector, Radiometer Input, is a socket type.

6.3.1 INPUT/OUTPUT INTERFACE SPECIFICATION

Presented below is a list of pin assignment for the five interface connectors. The characteristics associated with each input/output pin is briefly described.



Connectors J1, J3, J5, are Input Connectors

Connectors J2, J4 are Output Connectors

FIGURE 6-7

Input/Output Connector Arrangement

TABLE 6-5

Input/Output Connectors

Connector	Number of Pins	Signals
J1	15 pin plug	Power inputs & commands
J2	9 pin socket	Output signals
J3	15 pin socket	Input signals
J4	37 pin socket	Telemetry and Bench Test Equip. Test Point
J5	9 pin plug	Input clock signals

Input Connector J1

Pin	Term	Characteristics
1	-24.5 RAD	Connected to the negative terminal of the satellite primary regulated supply. To be used by the Radiometer.
2	-24.5 DRA	Connected to the negative terminal of the satellite primary regulated supply. To be used by the Radiometer Drive Amplifiers.
3	----	Spare Pin
4	OFFCMD	65 ms pulse with a nominal amplitude of +12 volts to the ON-OFF Relay. Input impedance is 160 ohms. Relay is turned off.
5	OFFCMDR	Relay OFF command return line
6	----	Spare Pin
7	GRD S	MRIR Signal Ground
8	GRD P	Power ground connected to the positive terminal of the satellite regulated supply.

Input Connector J1 (continued)

Pin	Term	Characteristics
9	-24.5 M	Connected to the negative terminal of the satellite primary regulated supply.
10	-24.5 TM	Connected to the negative terminal of the satellite primary regulated supply. To be used by the thermistor. Input impedance is nominal 2K ohms.
11	ONCMD	65 ms pulse with a nominal amplitude of +12 volts to the ON-OFF Relay. Input impedance is 160 ohms. Relay is turned on.
12	ONCMDR	Relay "ON" Command return line
13	----	Spare Pin
14	GRD T	Telemetry Ground
15	GRD C	Chassis Ground

Output Connector J2

Pin	Term	Characteristics
1	TRO 1	Tape Recorder Output No. 1 amplitude is +6.5 volts to +5.0 volts for the high state and 0 volts ± 0.6 volts for the low state. Output impedance is 330 ohms.
2	----	Spare Pin
3	GRD TRO 1	Tape Recorder Output No. 1 reference ground
4	GRD TRO 2	Tape Recorder Output No. 2 reference ground
5	GRD P	Power Ground
6	TRO 2	Tape Recorder Output No. 2 characteristics are same as TRO 1, Pin 1.
7	GRD S	Signal Ground
8	GRD T	Telemetry Ground
9	GRD C	Chassis Ground

Input/Output Connector J3

Pin	Term	Characteristics
1	-24.5 RAD	Negative terminal of the satellite primary regulated supply. Primary power is routed through the MRIR Unit to the Radiometer.
2	-24.5 RDA	Negative terminal of the satellite primary regulated supply. Primary power is routed through the MRIR Unit to the Radiometer Driver Amplifier.
3	----	Spare Pin
4	CH 1	Radiometer Analog Input No. 1 voltage amplitude is 0 volts to -6.4 volts at a frequency up to 8 cps. Input impedance is greater than 150K ohms when the analog gate is on.
5	CH 2	Radiometer Analog Input No. 2 (Same description as Pin 4.)
6	CH 3	Radiometer Analog Input No. 3 (Same description as Pin 4.)
7	GRD S	Signal Ground

Input/Output Connector J3 (continued)

Pin	Term	Characteristics
8	GRD P	Power Ground connected to positive terminal of the satellite primary regulated supply.
9	100 ØA	Output Phase A of a 2-phase, 100 cps square wave signal which is routed through the MRIR Unit to the Radiometer. Amplitude is -1.5 ± 1.0 volt for the high level and -23.0 ± 1.5 volts for the low level.
10	100 ØB	Output Phase B of a 2-phase, 100 cps square signal which is routed through the MRIR Unit to the Radiometer. Phase B leads Phase A by 90°. Amplitude same as Phase. B.
11	----	Spare
12	CH 4	Radiometer Analog Input No. 4 (Same description as Pin 4.)
13	CH 5	Radiometer Analog Input No. 5 (Same description as Pin 4.)
14	GRD T	Telemetry Ground
15	GRD C	Chassis Ground

Output Connector J4

Pin	Term	Characteristics
1	RLY TP	Relay Telemetry Point Output Voltage amplitude for ON condition is 8 ± 1.5 volts and 0 ± 0.6 volts for the OFF condition. Output impedance is 16.3K ohms.
2	TEM TP	Temperature Telemetry Point Output. Voltage amplitude is variable between -1.3 volts and -3.0 volts over the temperature range of -10°C to +65°C. Output impedance is less than 3K ohms over the temperature range. The output voltage is derived from a separate -24.5 volt supply.
3	----	Spare
4	-18V TP	MRIR -18 volts ±3 percent regulated secondary supply. Provided as monitor point. Provides 4.7K ohm isolation resistor on output.
6	-6V TP	MRIR -6 volts ±3 percent regulated secondary supply. Provides 4.7K ohm isolation resistor on output.
7	+6V	MRIR +6 volts ±3 percent regulated secondary supply. Provides 4.7K ohm isolation resistor on output.

Output Connector J4 (continued)

Pin	Term	Characteristics
8	+3.2V	MRIR +3.20 (+0.22V, -0.10V) regulator secondard supply. Provides 4.7K ohm isolation resistor on output.
9	-----	Spare
10	B4	208 cps symmetrical square wave output. Amplitude is +0.2 ± 0.1 volts for the "1" state and +2.0 ± 0.5 volts for the "0" state. Output impedance is greater than 4.7K ohms.
11	$\overline{B5}$	Pulse output that occurs every 4.8 milliseconds. Pulse duration for "2" state (+0.2 ± 0.1 volts) is 100 microseconds. For the remainder of the time, the "0" state is +2.0 ± 0.5 volts. Output impedance is greater than 4.7K ohms.
12	B1	1.66KC symmetrical square wave output. Amplitude for "1" state is +0.2 ± 0.1 volt and +2.0 ± 0.5 volts for the "0" state. Output impedance is greater than 4.7K ohms.

Output Connector J4 (continued)

Pin	Term	Characteristics
13	N4 (ECD)	20 microsecond pulse output which repeats every 4.8 milliseconds. Output amplitude is +0.2 ± 0.1 volts for the "1" state and +2.0 ± 0.5 volts for the "0" state. Output impedance is greater than 4.7K ohms.
14	$\overline{K4}$	25KC symmetrical square wave output with an amplitude of +2.0 ± 0.5 volts for the high level and +0.2 ± 0.1 volts for the low level. The output impedance is greater than 4.7K ohms.
15	C6	Pulse output that repeats 33 times per second pulse duration is 4.8 milliseconds. Voltage amplitude is +2.0 ± 0.5 volts for the "0" level and +0.2 ± 0.1 volts for the "1" level. The output impedance is greater than 4.7K ohms.
16	C1	Pulse output which occurs 30 milli-seconds after C6 occurs. The voltage amplitude and output impedance characteristics are the same as C6 on Pin 15.
17	-----	Spare Pin

Output Connector J4 (continued)

Pin	Term	Characteristics
18	GRD S	Signal Ground
19	GRD P	Power ground connected to the positive terminal of the satellite primary regulated supply.
20	-12 TP	-12 volt telemetry point output. Nominal voltage output is -6 volts ± 4 percent. The output impedance is 2.8K ohm ± 2 percent.
21	----	Spare Pin
22	$\overline{D1}$	LSB from the A/D Data Register. Voltage amplitude is +2.0 ± 0.5 volts for the "0" state and +0.2 ± 0.1 volts for the "1" state. Output impedance is greater than 4.7K ohms. Digital value is 2^0.
23	$\overline{D2}$	2^1 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
24	$\overline{D3}$	2^2 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.

Output Connector J4 (continued)

Pin	Term	Characteristics
25	$\overline{D4}$	2^3 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
26	$\overline{D5}$	2^4 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
27	$\overline{D6}$	2^5 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
28	$\overline{D7}$	2^6 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
29	D8	2^7 Digital bit from the A/D Data Register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
30	----	Spare Pin

Output Connector J4 (continued)

Pin	Term	Characteristics
31	COMP OT	Comparator output voltage. Voltage output swings from +3.0 volts for $V_{ladder} < V_{input}$ to -6.0 volts for $V_{ladder} > V_{input}$. Output impedance is greater than 4.7K ohms.
32	PREC V	Precision voltage output - to be determined.
33	ALOG INPT	A/D Ladder analog output to comparator. Voltage is variable from 0 to -6.4 volts nominally. Output impedance is greater than 4.7K ohms.
34	----	Spare pin
35	----	Spare pin
36	GRD T	Telemetry ground
37	GRD C	Chassis ground

Input Connector J5

Pin	Term	Characteristics
1	10KC CLK	10KC symmetrical square wave input nominal voltage swing is 0 volts to -6 volts. Input impedance is 3.3K ± 2 percent.
2	----	Spare
3	200 KC CLK	200KC symmetrical square wave input. Nominal voltage swing is 0 volts to -6 volts Input DC impedance is 5.1K ± 2 percent.
4	GRD 200 KC	Provided as 200KC input reference ground.
5	GRD P	Power ground connected to the positive terminal of the satellite primary regulated supply.
6	100 ØA	Input Phase A 100 cps square wave to be used by the Radiometer subsystem. Nominal voltage swing is same as J3, Pin 9.
7	100 ØB	Input Phase B 100 cps square wave to be used by the Radiometer subsystem. Nominal voltage swing is same as J3, Pin 10. Phase B leads Phase A by 90°.

Input Connector J5 (continued)

Pin	Term	Characteristics
8	-----	Spare pin
9	GRD S	Signal ground

6.4 PRINTED CIRCUIT BOARD MODULE TESTS

Each printed circuit board, after fabrication and assembly, will be submitted to a comprehensive static and semidynamic test. Since each integrated circuit used on the modules has been individually tested in accordance with the manufacturer's specifications, temperature cycled, and retested, it is felt that a go-no-go test will be sufficient to test the IC's on each module. Before a go-no-go test is performed, a thorough check of the PCB module is undertaken. Visual inspection is made to determine the quality of workmanship in soldering and etched circuit lines as well as correct placement of components. Continuity tests shall be performed between ground and voltage pins prior to applying power. A power dissipation test is made to see if excessive or too little power is being used, then the PCB module is subjected to the functional test.

Ground rules to support the go-no-go testing philosophy are presented herein.

a. Incorporate into each PCB test points which can be probed to provide pertinent data.

b. Break cyclic or long chains of logic by taking lines off the PCB. The chains can be "relinked" at the PCB interface connector.

c. Contain on each PCB that logic which provides a complete function.

Networks on modules which generate, shape, or amplify signals shall be tested for rise and fall times, distortion, and threshold values.

The PCB modules to be tested are as follows:

a. Analog Input - 25kc Generator

b. Encode - Timing Generator

c. Frame Sync Generator - Data Output

d. Analog/Digital Controller

e. Analog/Digital Converter

f. Primary Power Regulator

g. Secondary Power Supplies

Electrical schematics of the PCB modules listed above are contained in Appendix B.

6.4.1 ANALOG INPUT - 25KC GENERATOR

This module contains two independent functions: the Analog Input Commutator and the 25kc Clock Generator. The Analog Input commutation is accomplished by a 5-flip-flop ring counter that sequentially selects each of the five analog input channels. The analog input signal is gated through a Field-Effect-Transistor (FET) to the A/D Comparator network. The testing of the Analog Inputs consists of single clocking the ring counter and observing the logical results. This test ensures correct logical interconnections.

Since the ring counter is used to select the analog input channels, the FET selection switches can be tested at the same time for voltage offset.

The 25kc generator portion of the module consists of an input filter, clock shaper, and a modulo eight binary counter which divides the 200kc input clock to the required 25kc clock. The

testing of this function includes four portions:

a. Input Filter

b. Clock Shaper (exclusive "OR" network)

x. Modulo 8 Counter

d. 25kc Clock Driver

The procedure for testing is as above; namely, statically and semidynamically. The semidynamic test will operate the IC's at clock rates slightly higher than normal operation. Output signals leaving the PCB will be provided with equivalent dummy loads ac and/or dc, if applicable, in order to simulate worst-case conditions. The signal responses at the PCB interfaces shall be tested fully.

6.4.2 ENCODE - TIMING GENERATOR

The Encode-Timing Generator PCB module provides the following signals: (1) 1.66kc (bit time), (2) 209 cps (Transfer pulse), and (3) Encode Pulse (Frame Sync Enable - A/D initialization). To provide these timing signals, this PCB module contains a modulo 3 counter, a modulo 16 counter, and a hybrid ring counter. The modulo 3 and modulo 16 counters divide the 10-kc input signal into the 1.66kc and 209 cps signals. The hybrid ring counter operates from the 209 cps and 25kc signals to provide the initializing Encode pulse.

This PCB contains all IC networks except for a filter-level shifter network for the 10kc input clock. The procedure for testing this module is similar to the procedure established for the analog input PCB. The clocks will be provided in single incremental steps, test points will be probed to determine if

logical levels are correct. After static testing, the module will be tested at its dynamic clock rate. Signals leaving the modules will be tested under load to ensure proper switching and amplitude characteristics.

6.4.3 ANALOG/DIGITAL CONVERTER TESTING

The Analog/Digital Converter PCB will be tested in more detail than the PCB's containing the Integrated Circuits. This is necessary if the requirement for the full range conversion accuracy over the temperature range of $-10^{o}C$ to $+60^{o}C$ is to be 0.375 percent. With full range being from 0 volts to -6.4 volts, the maximum allowable error is ±12.5 millivolts or ±1/2 bit.

The testing of the A/D Converter can be performed under static and dynamic conditions. The static test will serve to check the following:

a. Precision Supply

b. Current Source Switches

c. Current Sources

d. Ladder Network Output

e. Analog Comparator Output

The precision supply will be tested from no load to full load conditions. Tolerances on noise, ripple, and stability of the precision supply shall be determined in conjunction with the overall error contribution of each part of the A/D conversion. The test points pertaining to the precision voltage and its reference, the ladder network output, and the analog comparator output are available at the PCB interface connector. These test

points shall be utilized to test the A/D Converter under low temperature, room temperature, and high temperature tests independently from the total MRIR Subsystem.

All aspects of the A/D shall be tested at room temperature. Each current source shall be selected independently (ON-OFF) and then together (turn on 1, turn on 2, etc.). The output of the ladder (test point V_L) shall be monitored by a DVM and/or a VTVM and the results checked and tabulated. After the room temperature test, a static test shall be performed at $-10^{\circ}C$ and $+60^{\circ}C$. The testing at these temperature extremes shall be more comprehensive in that all 256 bits shall be resolved. During the testing, the analog output, ladder output, precision voltage, and precision voltage reference shall be continually monitored and the results tabulated. All results shall be within tolerances established to provide an A/D conversion at the accuracy required.

The offset voltage error of the ladder and comparator amplifier shall be tested by adjusting the analog input until a change occurs at the comparator output. The ladder extension network shall be adjusted to provide a minimum error.

No dynamic testing shall be performed at the individual PCB level. The dynamic testing shall be accomplished when the MRIR Telemetry Unit is tested as a complete system by the Bench Test Equipment.

6.4.4 POWER SUPPLY TESTING

The power supply consists of two PCB modules. These two modules shall be tested together. The tests to be performed shall consist of the following:

a. ON-OFF Relay

b. Telemetry Points

c. Primary Power Pre-regulator

   (1) Primary Power High

   (2) Primary Power Low

d. Secondary Levels

   (1) No-load regulation

   (2) Half-load regulation

   (3) Full-load regulation

   (4) Ripple

   (5) Noise

   (6) Modulation

   (7) Maximum Δ V

All tests on the power supply shall be performed at room temperature, low temperature ($-10^{o}C$), and high temperature ($+60^{o}C$).

6.4.5 ANALOG/DIGITAL DATA CONTROL TESTING

The A/D Data Control PCB module provides the logic to perform the successive approximation technique in this analog-to-digital converter. The module contains all IC's with the exception of isolation test point resistors which provide short circuit

protection. The PCB contains a shift register, data conversion register, comparator reset gates, and the Frame Sync word inhibit gates.

The shift register establishes the sampling rate by sequentially selecting a corresponding data register flip-flop. The comparator reset gates will reset the selected data register flip-flop if the voltage of the ladder network (V_L) is greater than the Analog Input Voltage (V_I)

The Frame Sync inhibit gates will prohibit the Frame Sync word from occurring as the result of a natrual A/D conversion. The Frame Sync word is 10111000. The Frame Sync inhibit will change the least significant bit to a one(1) if the Frame Sync word format were to appear. Negation tests through flip-flop control of the data register will ensure proper operation of the inhibit gates.

The testing of this PCB will be performed on a go-no-go basis under static and dynamic conditions. To provide a more complete dynamic test, this board shall be tested with the A/D in the overall MRIR system test. Otherwise, the dynamic testing will be rather complex if actual operating conditions are to be provided.

6.4.6 MRIR TELEMETRY UNIT SUBSYSTEM TEST

6.4.6.1 General

A test procedure necessary to determine that the MRIR-PCM Digital Electronics Subsystem is functioning properly is presented herein. The testing will be performed with the subsystem being considered as a black box. The only signals available

for testing are supplied through the connectors. Continuity, frequency, and voltage measurements are included in the tests.

6.4.6.2 Continuity Tests

Continuity tests will be performed on wires that are routed through the box, such as the 100 cps, phase A. Also a check shall be made for chassis isolation from signal ground.

6.4.6.3 Power ON-OFF Relay

The power ON-OFF relay is controlled by two push button switches. When the relay is in the "ON" position, an indicator will be illuminated. This indicator will be controlled by the telemetry relay signal.

6.4.6.4 Voltage Measurements

The following subsystem DC/DC Converter voltages shall be measured for their respective values.

Voltage	Reading
-18v	-18.0 ± 0.54 vdc
-12v	-12.0 ± 0.36 vdc
-6v	-6.0 ± 0.18 vdc
+6v	+6.0 ± 0.18 vdc
+3.2v	+3.2 +0.22, - 0.1 vdc
D/A volt	To be determined

6.4.6.5 Frequency Measurement

The following frequencies shall be monitored for proper operation. These measurements will indicate the proper frequency division of the flip-flops in a chain.

Term	Measurement
B1	1.66 kc
B4	208 cps
B5'	100μs pulse at 205 cps
K4'	25 kc

6.4.6.6 Power Measurement

The power required to operate the subsystem is obtained by measuring the drop across a series resistor in the power input lines. The current required should be less than 100 milliamperes. Also, the power supply shall be tested to ensure that less than 250 millivolts peak-to-peak noise is fed back on the primary line.

6.4.6.7 Channel Encoding and Interference Tests

This test shall verify that each input channel is being sampled and encoded. The operation consists of five analog signals, with each one a different value to a channel. The signals are sampled and encoded in the MRIR A/D Converter. The digital output is then decoded in the Bench Test Equipment to form a stairstep wave. Varying each Radiometer input will verify its position in the scope waveform. The presence of interference between channels will then be indicated on the scope.

6.4.6.8 Dynamic Channel Selection and Encoding Test

The following section is to determine that the subsystem samples each channel properly and inserts it correctly into the serial output.

A function generator is used to supply a 6.4 ± 0.2 volts peak-to-peak signal to one of the input channels. The serial output is decoded in the Bench Test Equipment to obtain an analog signal. A scope display will show the function generator output on one channel and a stairstep approximation on the other channels. Varying the function generator timing between 1 cps and 8 cps, the decoded output from the Bench Test Equipment should follow the square wave. This operation is repeated for all channels.

6.4.6.9 Analog Input Repeatability Test

This section is to verify that each sample of an unvarying input is encoded identically.

The operation consists of comparing the decoded output from the subsystem with a fixed value in the Bench Test Equipment. Each time a disagreement occurs, a counter in the Bench Test will be incremented once. If the A/D Converter is working properly, the counter will remain at zero. The above test is repeated for all channels.

6.4.6.10 A/D Converter Calibration

The following section is to calibrate the linearity of the A/D Converter.

A voltage source set at zero is connected to Radiometer input channel 1. The encoded output from the subsystem A/D Converter is loaded into a register in the Bench Test Equipment which displays each bit on neon indicators.

By increasing the input voltage to channel 1, each succeeding neon (LSB to MSB) will illuminate. At the time of illumination, the bit will correspond to the input voltage.

6.4.6.11 Analog Gate Leakage Test

The following section is to measure any excess leakage currents presented by the analog switches in the subsystem. Since FET circuitry is used in the analog gates, no d-c offset should be present.

This test will require that a voltage source be applied to one of the channel inputs. One shot the subsystem ring counter until the gate under test is switched on. When the channel input is measured using the subsystem A/D analog input line as a reference, the reading will be less than 3 millivolts. The above test is then repeated for all channels.

6.4.6.12 Analog Gate Input Current

This section is to measure the input current drawn by the subsystem analog gates.

A voltage source of -3.000 ± .001 volts is applied to one of the input channels through a 100K series resistor. A DVM is used to measure the drop across the series resistor. The current shall be less than 1 microampere.

This test is then repeated for all channels.

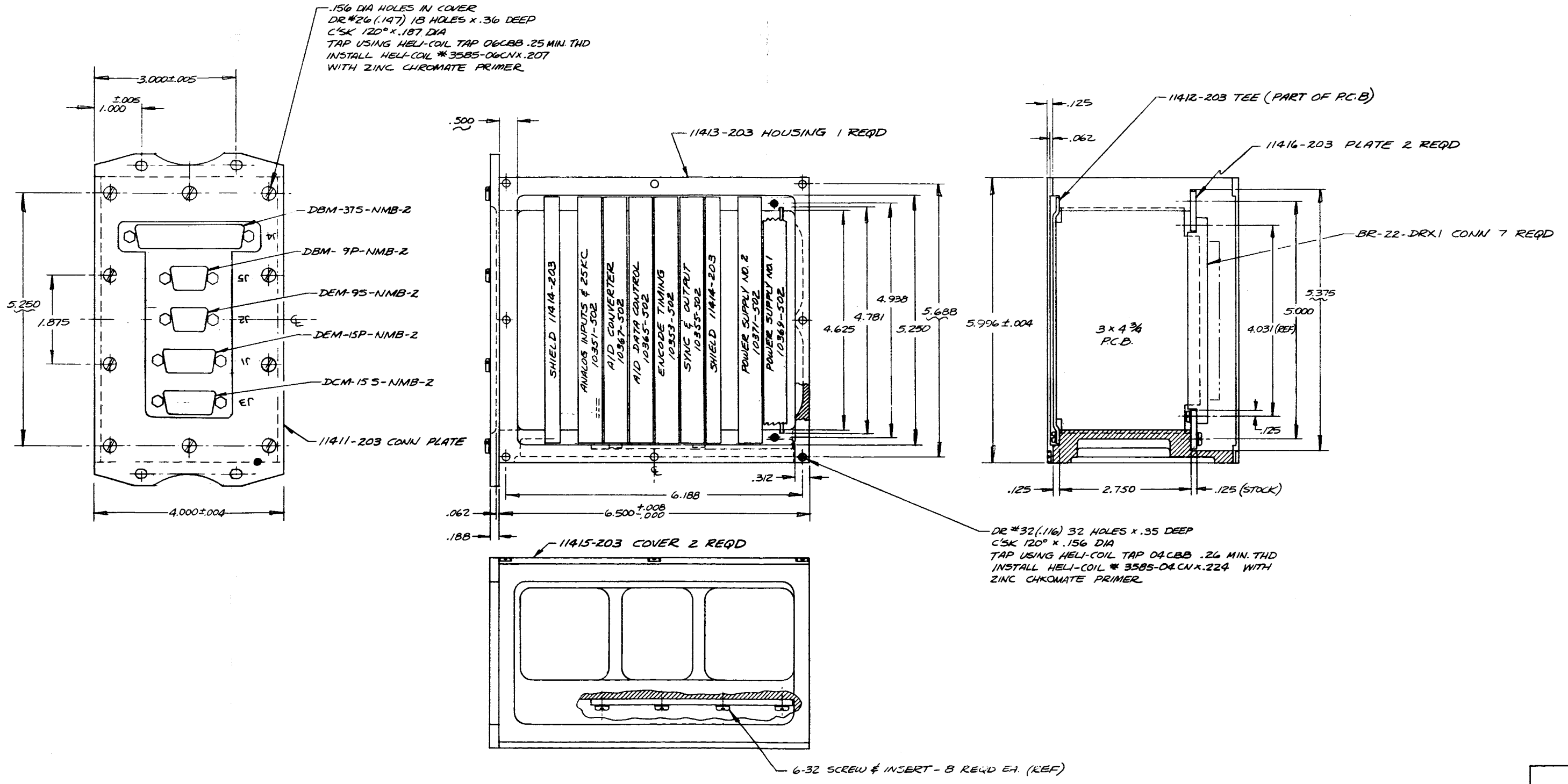
6.4.6.13 Telemetry Outputs

The following telemetry signals for the subsystem will be measured and recorded.

Signal	Reading
TEM TP	Between 0 and -6 volts
-12V TP	-6 ± 0.25 volts dc
RLY TP	-8v ± 1 volts dc

APPENDIX A

MECHANICAL DRAWINGS



LAYOUT — MRIR-PCM
DIGITAL SUB-SYSTEM

B. HENEGAR 11-10-3 | 910015-102

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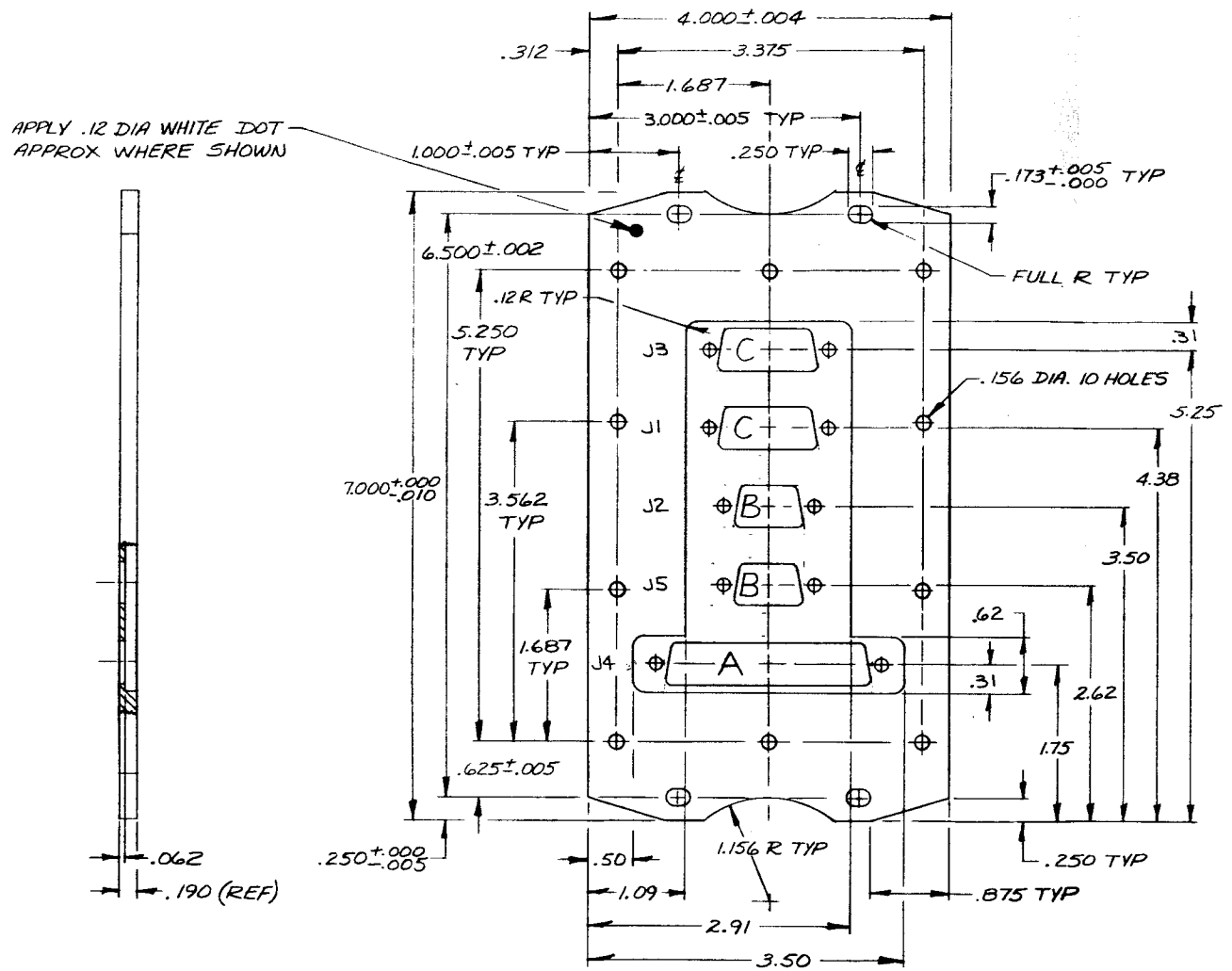

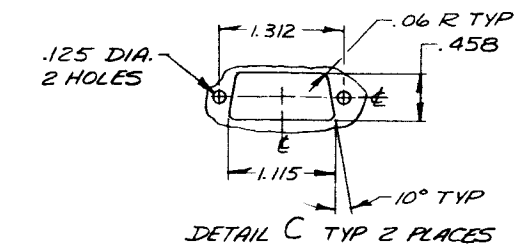

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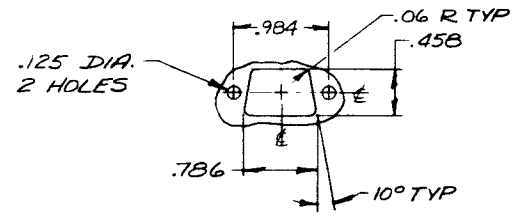

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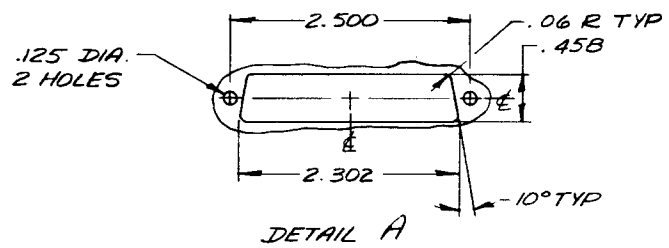

DETAIL A

5. TAG WITH PART NO PER CCP SPEC A0104-001
4. $\sqrt{23}$ ALL MACHINED SURFACES
⟨1⟩ 3. DOW #17 PER MIL-M-45202 TYPE 1, CLASS C
2. RUBBER STAMP DESIG. APPROX WHERE SHOWN PER CCP SPEC A0104-001 USING BLACK INK.
1. MACHINE PER CCP SPEC A0102-001

NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	11411-203	CONN. PLATE	.190 × 4.06 × 7.06 AZ31B-H24 MAG. ALY QQ-M-44	

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED			
DIMENSIONS ARE IN INCHES	DRAWN	D. MILLER	12-28-65
TOLERANCES ON	CHECK		
DECIMALS .XX ±.03 .XXX ±.010 / ANGLES ± 0° 30'	APPD		
	APPD		
DRILLED HOLES	FINISH	⟨1⟩	
.040 TO .1285: +.002, —.001			
.136 TO .228: +.003, —.001			
.234 TO .500: +.004, —.001			
.515 TO .750: +.005, —.001	HEAT TREAT		
.765 TO 1.000: +.007, —.001			
1.015 TO 2.000: +.010, —.001	SURFACE ROUGHNESS PER MIL-STD-10	✓	

DO NOT SCALE THIS DRAWING

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

CONN. PLATE MRIR-PCM

SCALE:	SIZE	
FULL	D	11411-203
WEIGHT	SHEET 1 OF 1	

REVISIONS			
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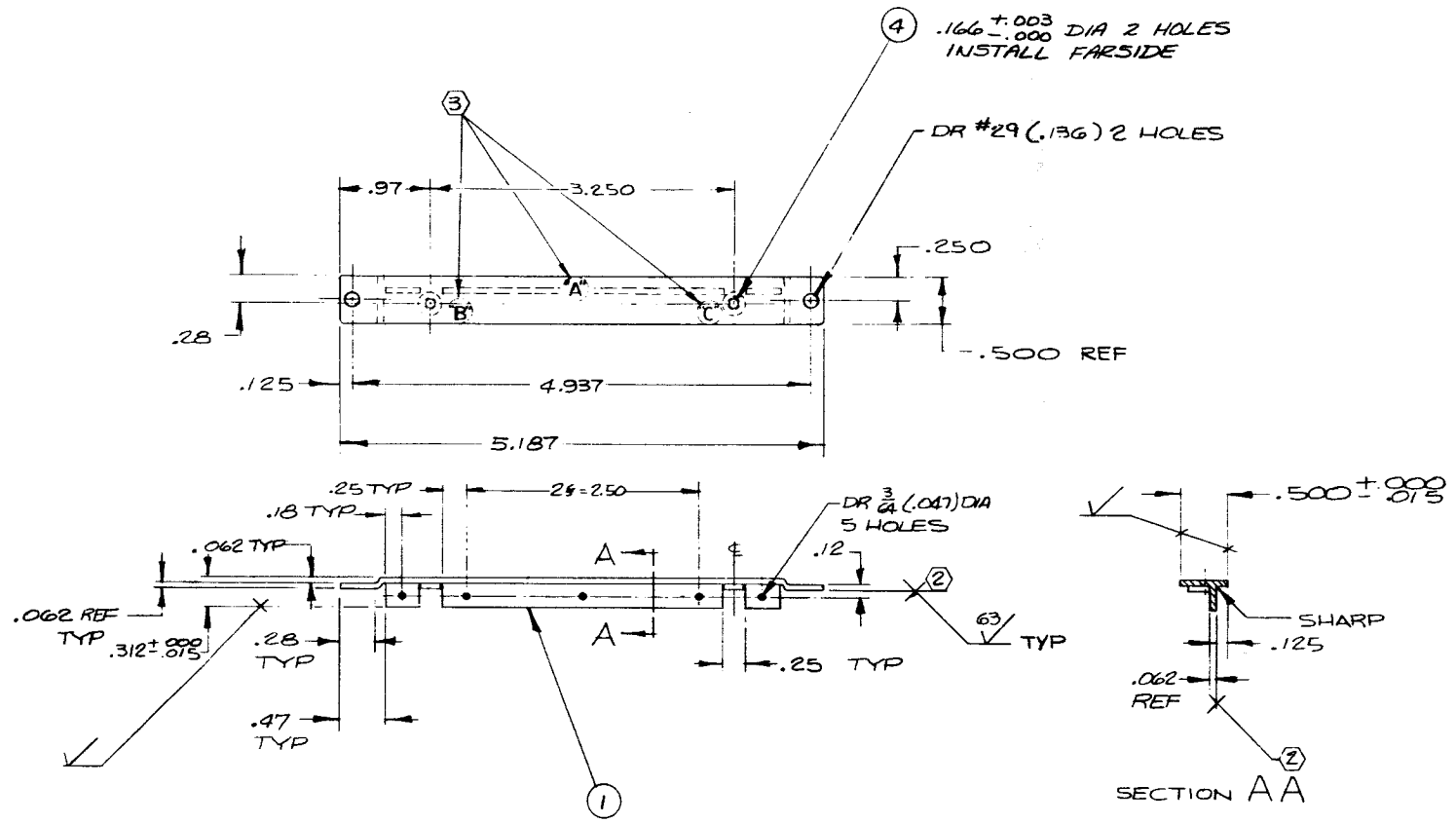
DASH NO	"A" (3)	"B" (3)	"C" (3)
-11	ANALOG INPUTS & 25KC	ASSY NO 10351-502	SERIAL NO (4)
-21	ENCODE-TIMING	ASSY NO 10353-502	SERIAL NO (4)
-31	FRAME SYNC & OUTPUT	ASSY NO 10355-502	SERIAL NO (4)
-41	A/D DATA CONTROL	ASSY NO 10365-502	SERIAL NO (4)
-51	A/D CONVERTER	ASSY NO 10367-502	SERIAL NO (4)
-61	POWER SUPPLY #1	ASSY NO 10369-502	SERIAL NO (4)
-71	POWER SUPPLY #2	ASSY NO 10371-502	SERIAL NO (4)



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									NOTE: UNLESS OTHERWISE SPECIFIED
									1. MACHINE PER CCP SPEC A0102-001.
									2. CAUSTIC DIP AFTER ELECTRO-ETCHING.
									3. BREAK SHARP EDGES .010-.015.
									4. NORMAL WITHIN .005 IN/IN. TYP BOTH ENDS.
									5. 125 ALL MACHINE SURFACES.
									6. ELECTRO-ETCH DESIGNATIONS APPROX WHERE SHOWN USING .10 HIGH CHARACTERS.
									7. TO BE ASSIGNED
									8.
									9. MAKE FROM PA 6530 X 5.25, 6063-T5 AL ALY EXT. PIONEER ALUM, LOS ANGELES, CALIFORNIA.
									10. PENN ENG'G & MFG CORP, DOYLESTOWN, PA.

ITEM NO	-71	-61	-51	-41	-31	-21	-11	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE
(6)	4	2	2	2	2	2	2	2	CLS-440-2	NUT, CLINCH		COML	
(5)	1	1	1	1	1	1	1	1	11412-203-1	TEE	(5)	(5) COML	
	1	1	1	1	1	1	1	1	11412-203	TEE, P.C.B.			

LIST OF MATERIAL OR PARTS LIST

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DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX ± .03 .XXX ± .010 ANGLES ± 0° 30'	CHECK		
	APPD		
	APPD		
DRILLED HOLES .040 TO .1285: + .002, — .001 .136 TO .228: + .003, — .001 .234 TO .500: + .004, — .001 .515 TO .750: + .005, — .001 .765 TO 1.000: + .007, — .001 1.015 TO 2.000: + .010, — .001	FINISH (1)		
	HEAT TREAT		
	SURFACE ROUGHNESS PER MIL-STD-10 ✓		

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

TEE-P.C.B. ASSY

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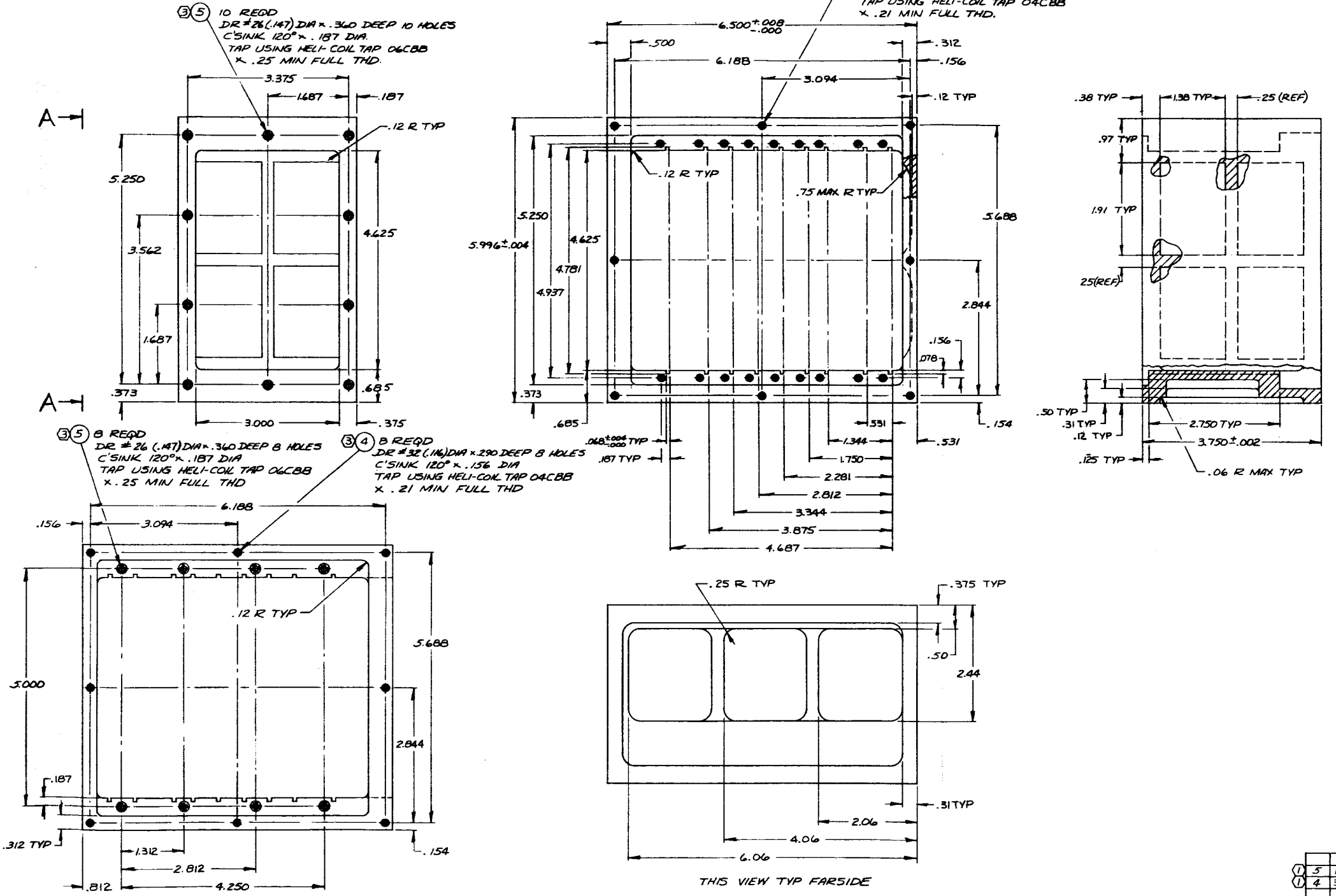

6. TAG WITH PART NO. PER CCP SPEC A0104-001
(3) 5. ZIP IN 2 N.C. CHROMATE PRIMER BEFORE INSTALLING.
4 4. 63 ALL MACHINED SURFACES
(2) 3. DOW #17 PER MIL-M-45202 TYPE I, CLASS C.
(1) 2. HELI-COIL CORP, DANBURY, CONN.
1. MACHINE PER CCP SPEC A0102-001
NOTE: UNLESS OTHERWISE SPECIFIED

ITEM	AJD	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	5	16	3585-04CN×.207	INSERT		COML
1	4	34	3585-04CN×.168	INSERT		COML
1		1	-3	HOUSING	9.00 DIA. x 3.81 ZK60A-T5 MAG. ALY	QQ-M-31
1		1	11413-203	HOUSING, P.C.B.		

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED	DRAWN: D. MILLER 12-9-65
DIMENSIONS ARE IN INCHES	CHECK
TOLERANCES ON DECIMALS .XX ± .03, .XXX ± .010; ANGLES ± 0° 30'	APPD
	APPD
DRILLED HOLES: .060 TO .128 ± .002 — .001; .136 TO .228 ± .003 — .001; .234 TO .358 ± .004 — .001; .363 TO .734 ± .005 — .001; .785 TO 1.000 ± .007 — .001; 1.055 TO 2.000 ± .008 — .001	FINISH (2)
	HEAT TREAT
	SURFACE ROUGHNESS PER MIL-STD-10 ✓

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

HOUSING P.C.B.
MRIR-PCM

SCALE: FULL. | SIZE: F | 11413-203

DO NOT SCALE THIS DRAWING | WEIGHT | SHEET 1 OF 1

REVISIONS				
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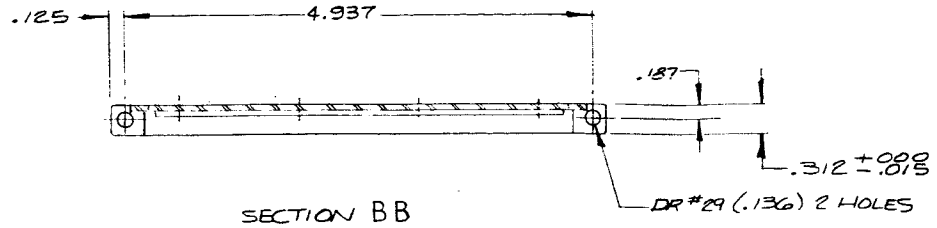

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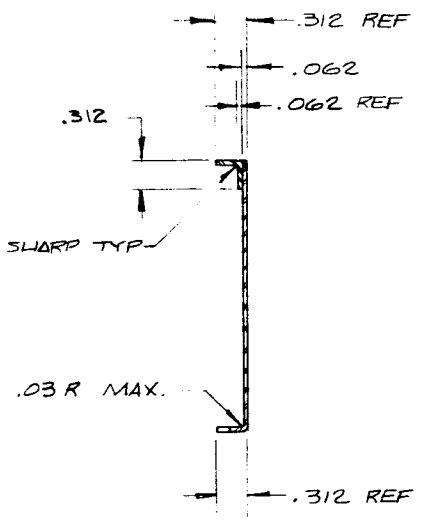

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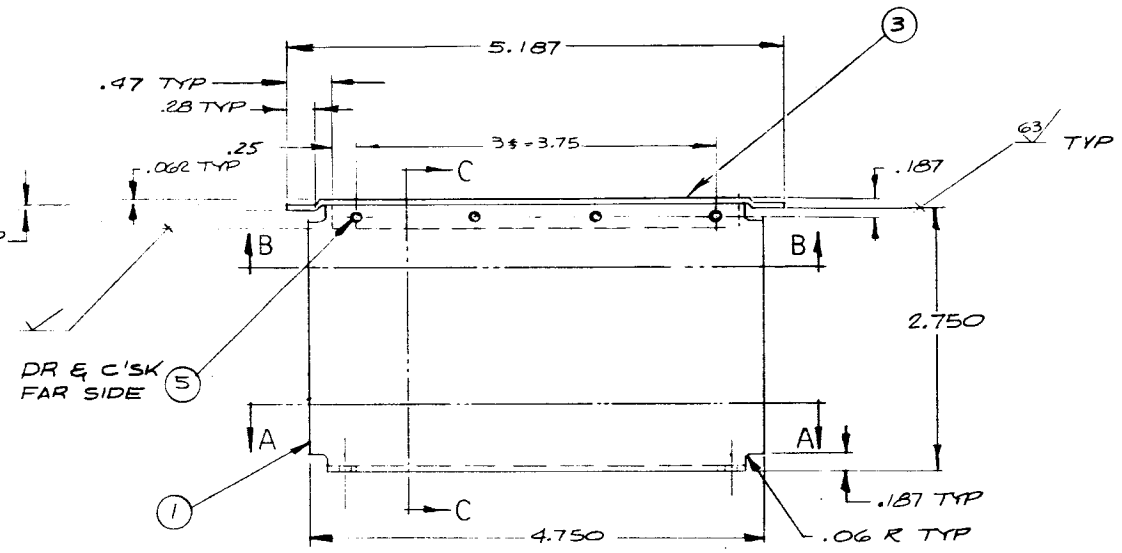

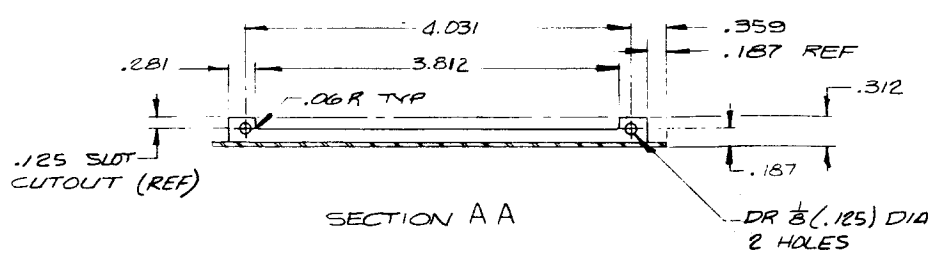

SECTION AA

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3	1	11414-203-5	TEE	(2)	(2)		
1	1	11414-203-3	SHIELD	.06 X 3.18 X 4.81	5052 H32 AL ALY SHT	QQ-A-318c	
	1	11414-203	SHIELD - PCB				

LIST OF MATERIAL OR PARTS LIST

7. IDENTIFY PER CCP SPEC A0104-001.
(2) 6. MAKE FROM PA 6530 X 5.25 6063-T-5 AL ALY EXT PIONEER ALUM, LOS ANGELES, CALIFORNIA.
5. 125 / ALL MACHINE SURFACES.
4. FABRICATE PER CCP SPEC A0103-001
3. BREAK SHARP EDGES .010 - .015.
(1) 2. CAUSTIC DIP..
1. MACHINE PER CCP SPEC A0102-001.
NOTE: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 0° 30'

DRILLED HOLES

.040	TO .1285	+.002, —.001
.136	TO .228	+.003, —.001
.234	TO .500	+.004, —.001
.515	TO .750	+.005, —.001
.765	TO 1.000	+.007, —.001
1.015	TO 2.000	+.010, —.001

DRAWN	A. R. COLL	12-30-65
CHECK		
APPD		
APPD		
FINISH	(1)	
HEAT TREAT		
SURFACE ROUGHNESS PER MIL-STD-10	✓	

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SHIELD - P. C. B. MRIR P.C.M.

SCALE:	SIZE	
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DO NOT SCALE THIS DRAWING	WEIGHT	SHEET

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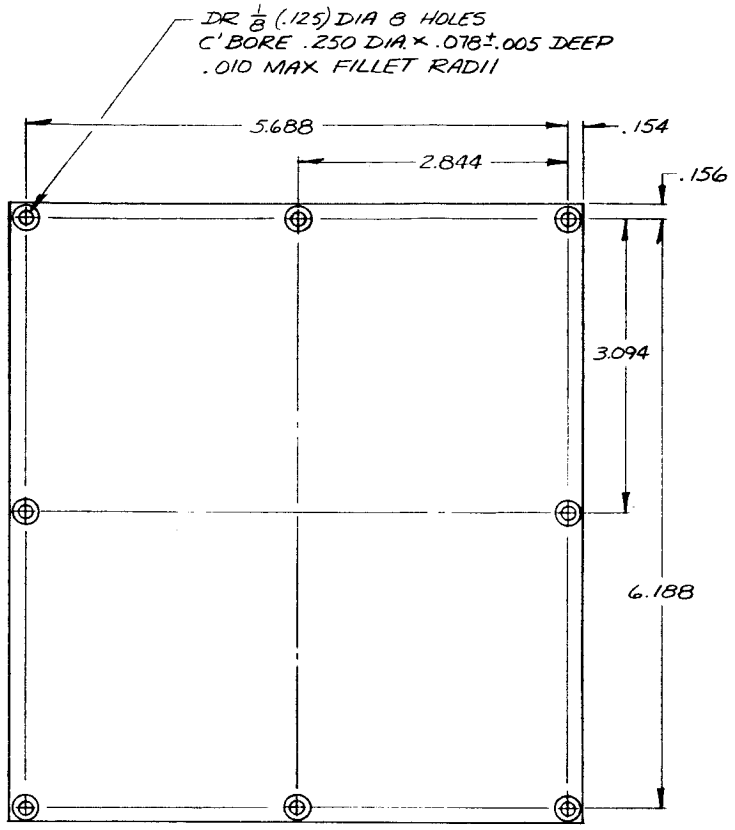
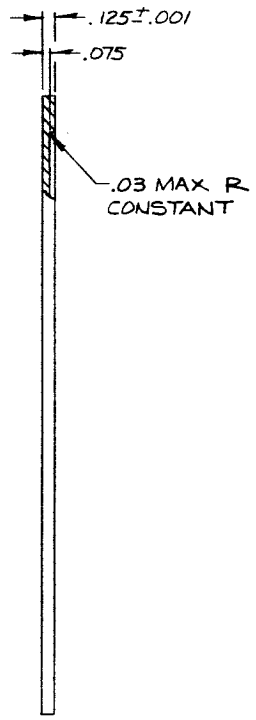
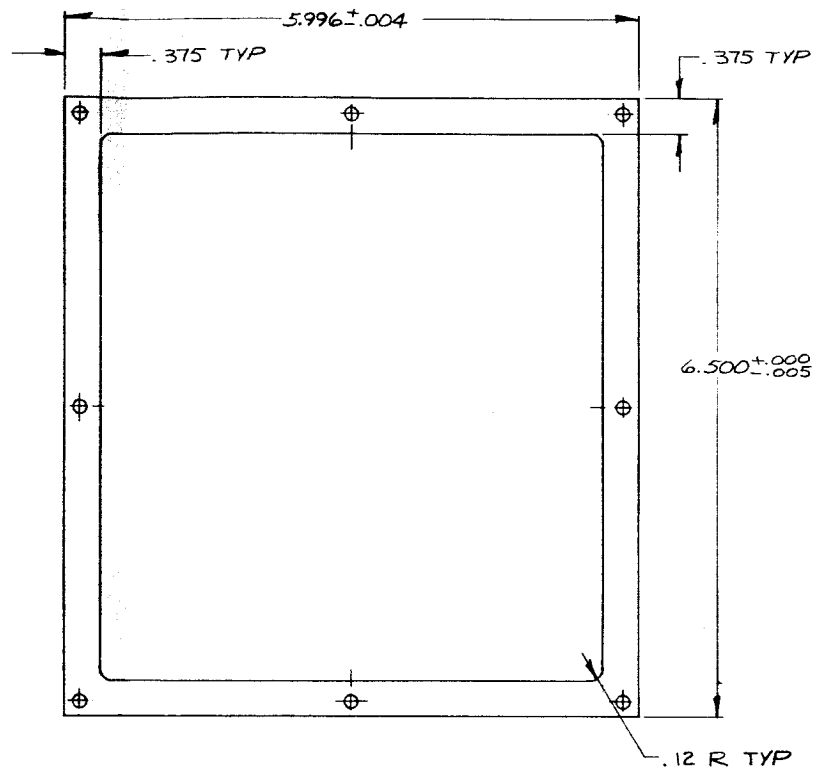






3. TAG WITH PART NO. PER CCP SPEC A0104-001
(1) 2. DOW #17 PER MIL-M-45202 TYPE I, CLASS C
1. MACHINE PER CCP SPEC A0102-001
NOTE: UNLESS OTHERWISE SPECIFIED

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	11415-203	COVER	.160 x 6.06 x 6.56 AZ31B-H24 MAG. ALY	QQ-M-44

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: .XX ± .03, .XXX ± .010
ANGLES: ± 0° 30'

DRILLED HOLES

.040	TO .1285	+.002, —.001
.136	TO .228	+.003, —.001
.234	TO .500	+.004, —.001
.515	TO .750	+.005, —.001
.765	TO 1.000	+.007, —.001
1.015	TO 2.000	+.010, —.001

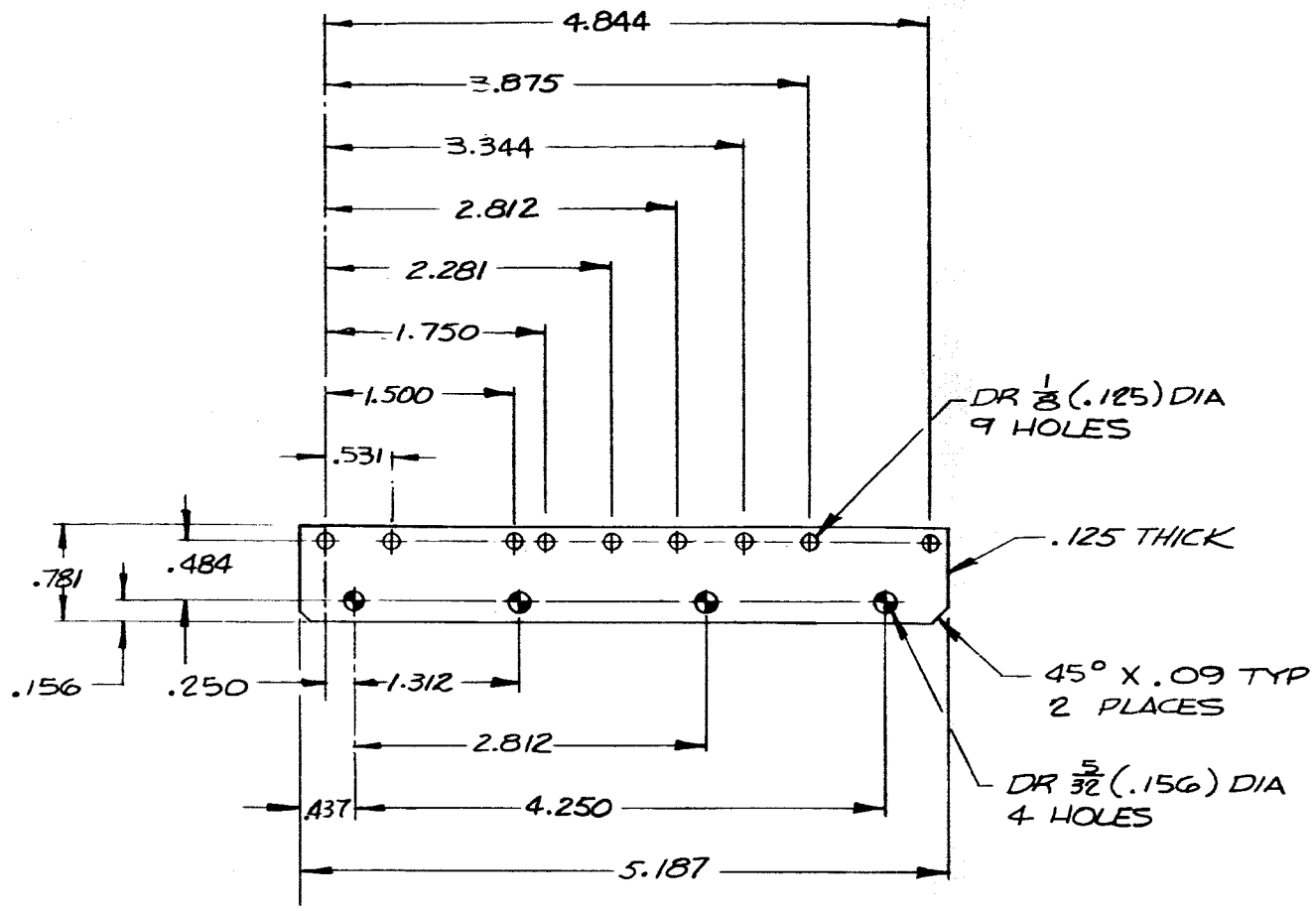
DRAWN	D. MILLER	12-29-65
CHECK		
APPD		
APPD		
FINISH	(1)	
HEAT TREAT		
SURFACE ROUGHNESS PER MIL-STD-10	✓	

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

COVER, HOUSING MRIR-PCM

SCALE:	SIZE	
FULL	D	11415-203
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET 1 OF 1

REVISIONS				
SYM	ZONE	DESCRIPTION		DATE & APPROVAL
		[1] MAY BE REWORKED [2] CANNOT BE REWORKED [3] NONE	DISPOS	CLASS



3. TAG WITH PART NO. PER CCP SPEC. A0104-001.
(1) 2. FINISH; DOW#17 PER MIL-M-45202, TYPE I, CLASS C.
1. MACHINE PER CCP SPEC A0102-001.
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	11416-203	PLATE-MTG	.125 X 5.875 X 5.250 AZ31B-H24 MAG. ALY	QQ-M-44

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: .XX ± .03, .XXX ± .010
ANGLES: ± 0° 30'

DRILLED HOLES

.040	TO .1285	+.002, —.001
.136	TO .228	+.003, —.001
.234	TO .500	+.004, —.001
.515	TO .750	+.005, —.001
.765	TO 1.000	+.007, —.001
1.015	TO 2.000	+.010, —.001

DRAWN	A.R. COLL	12-30-68
CHECK		
APPD		
APPD		
FINISH	(1)	
HEAT TREAT		
SURFACE ROUGHNESS PER MIL-STD-10	✓	

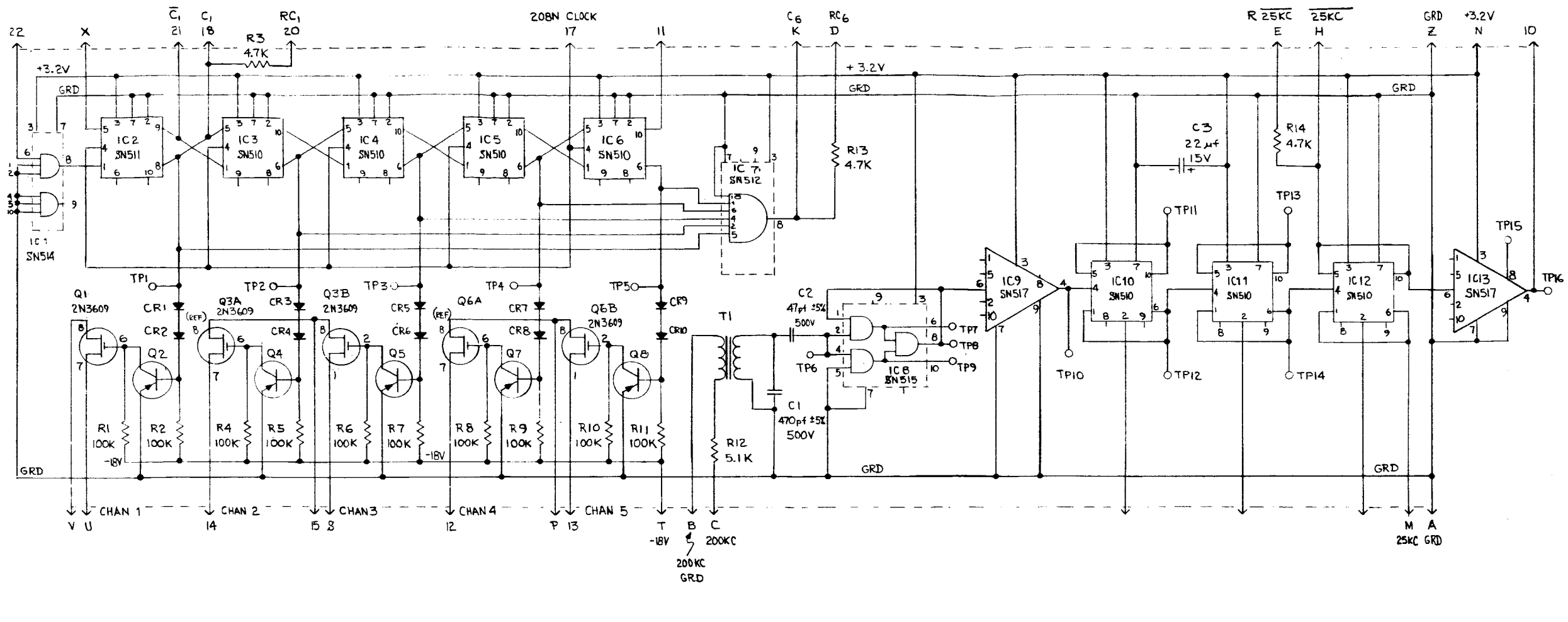
CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

PLATE—MTG. CONN. MRIR—PCM

SCALE:	SIZE	
1	C	11416-203
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET

APPENDIX B

ELECTRICAL SCHEMATICS



3. ALL RESISTORS VALUES ARE ±2% ¼W
2. ALL DIODES ARE
1. ALL TRANSISTORS ARE 2N2604
NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	10350-502	SCHEMATIC		

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: .XX ± .03, .XXX ± .010 | ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .1285: +.002, —.001
.136 TO .228: +.003, —.001
.234 TO .500: +.004, —.001
.515 TO .750: +.005, —.001
.765 TO 1.000: +.007, —.001
1.015 TO 2.000: +.010, —.001

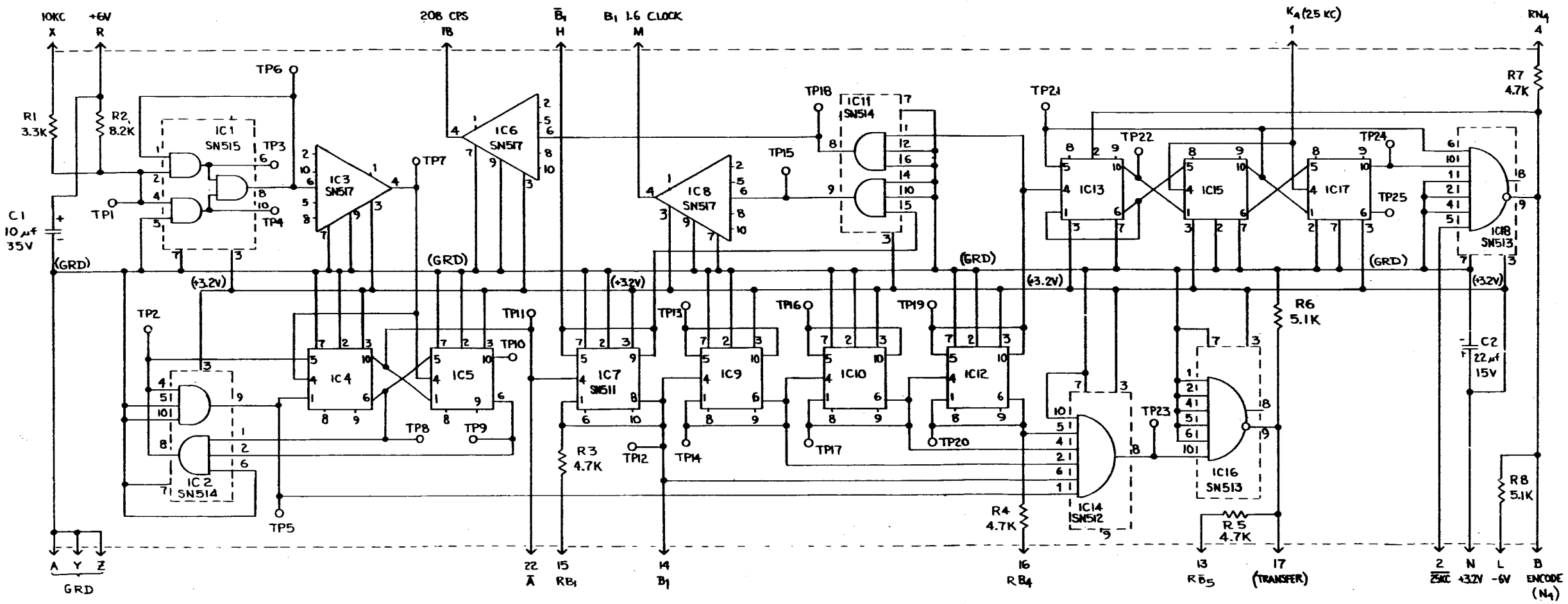
DRAWN	O. HAMPTON	12-6-65
CHECK		
APPD		
APPD		
FINISH		
HEAT TREAT		
SURFACE ROUGHNESS PER MIL-STD-10	✓	

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC— ANALOG INPUTS & 25 KC GENERATOR

SCALE: NONE | SIZE: D | 10350-502
DO NOT SCALE THIS DRAWING | WEIGHT | SHEET

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REVERSED 2 CANNOT BE REVERSED 3 NONE	



3. REFERENCE ASSY DWG NO. 10353-502
2. ALL RESISTORS ARE ±2% ¼W
1. ALL INTERGRATED CIRCUITS ARE SN510
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1	10352-502	SCHEM		

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: XX ± .03, XXX ± .010
ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .128 ± .002, — .001
.136 TO .228 ± .003, — .001
.234 TO .500 ± .004, — .001
.515 TO .750 ± .005, — .001
.765 TO 1.000 ± .007, — .001
1.015 TO 2.000 ± .010, — .001

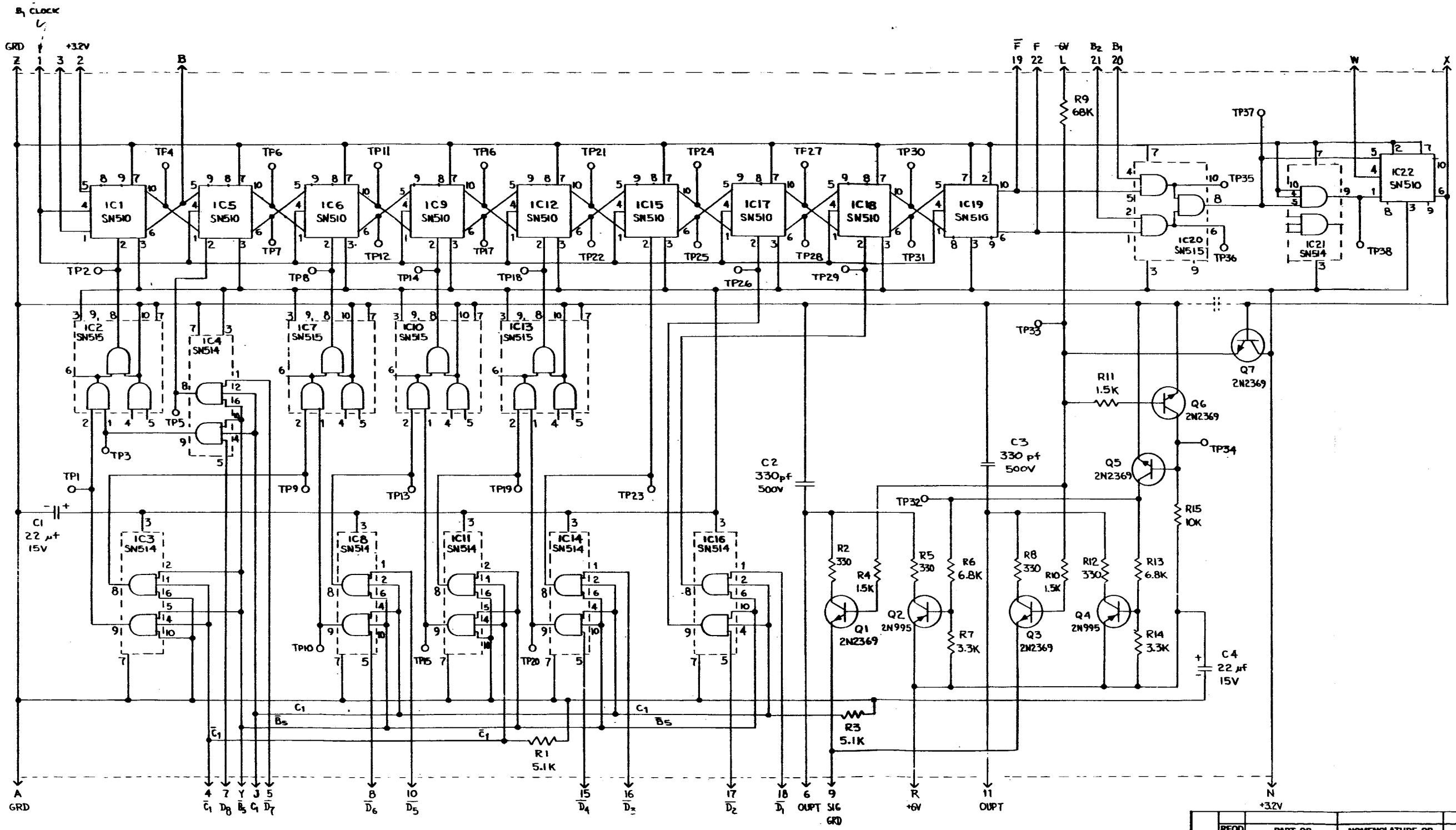
DRAWN O. HAMPTON 12-9-65
CHECK
APPD
APPD
FINISH
HEAT TREAT
SURFACE ROUGHNESS PER MIL-STD-10 ✓

CALIFORNIA COMPUTER PRODUCTS INC.
385 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC - ENCODE-TIMING GENERATOR

SCALE: NONE
SIZE: D
10352-502
DO NOT SCALE THIS DRAWING
WEIGHT
SHEET

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REORDERED 2 CANNOT BE REORDERED 3 NONE	



1. RESISTOR VALUES ARE ±2% ¼W
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: XX ± .03, XXX ± .010
ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .1285: +.002, -.001
.136 TO .228: +.003, -.001
.234 TO .500: +.004, -.002
.515 TO .750: +.005, -.002
.765 TO 1.000: +.007, -.001
1.015 TO 2.000: +.010, -.001

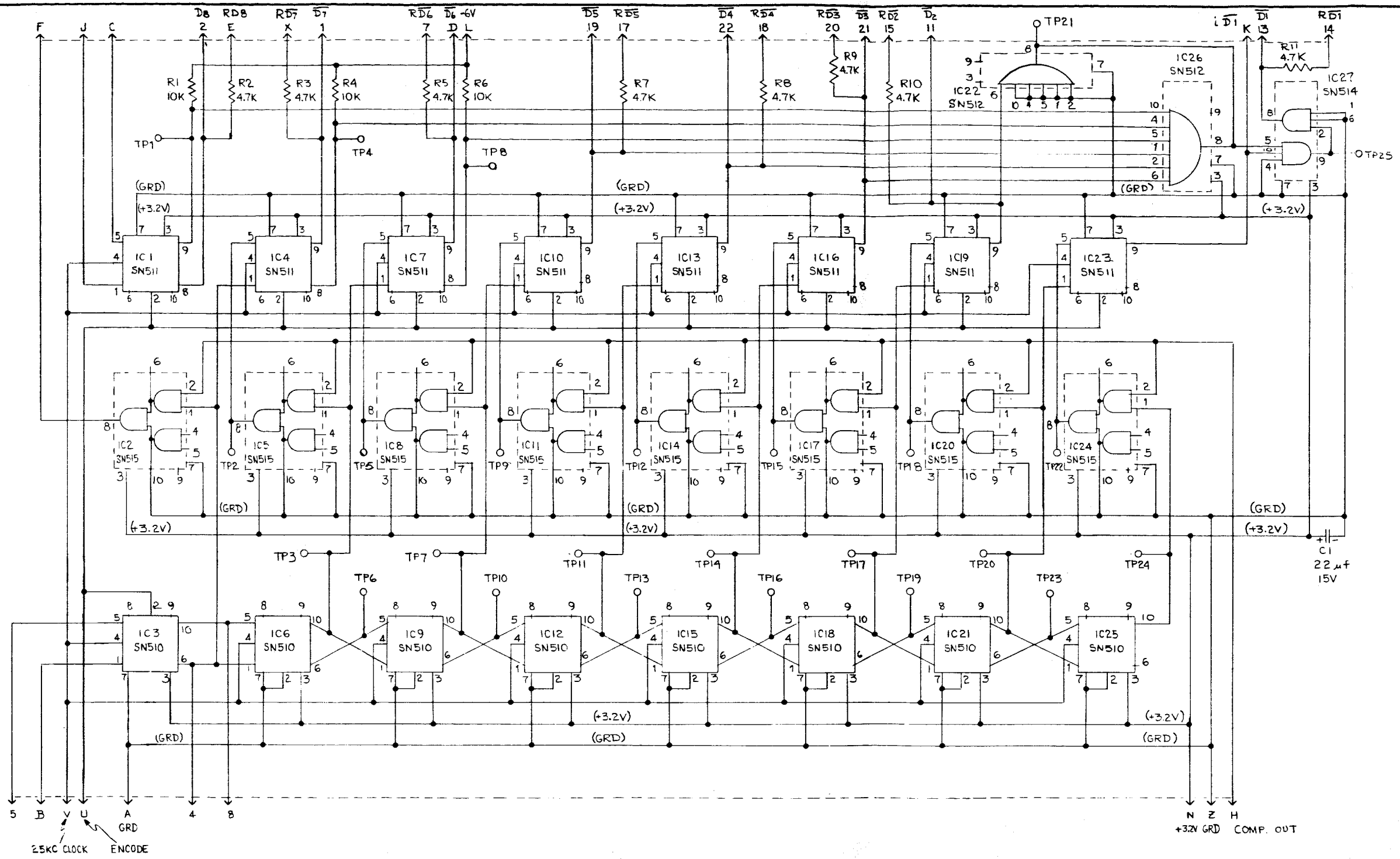
DRAWN	O. Hampton	20 Dec 65
CHECK		
APPD		
APPD		

FINISH
HEAT TREAT
SURFACE ROUGHNESS PER MIL-STD-10 ✓

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC-
FRAME SYNC & DATA OUPT

SCALE:	SIZE	
NONE	D	10356-502
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET



REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	

2. REF ASSY DWG NO. 10365-502
1. RESISTOR VALUES ARE ±2% ¼W
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
1		SCHEMATIC		

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS .XX ± .03 .XXX ± .010
ANGLES ± 0° 30'
DRILLED HOLES
.040 TO .128 ± .002, — .001
.136 TO .228 ± .003, — .001
.234 TO .500 ± .004, — .001
.515 TO .750 ± .005, — .001
.765 TO 1.000 ± .007, — .001
1.015 TO 2.000 ± .010, — .001

DRAWN O. HAMPTON 18 DEC 1965
CHECK
APPD
APPD
FINISH
HEAT TREAT
SURFACE ROUGHNESS PER MIL-STD-10 ✓

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC - ANALOG TO DIGITAL DATA CONTROL

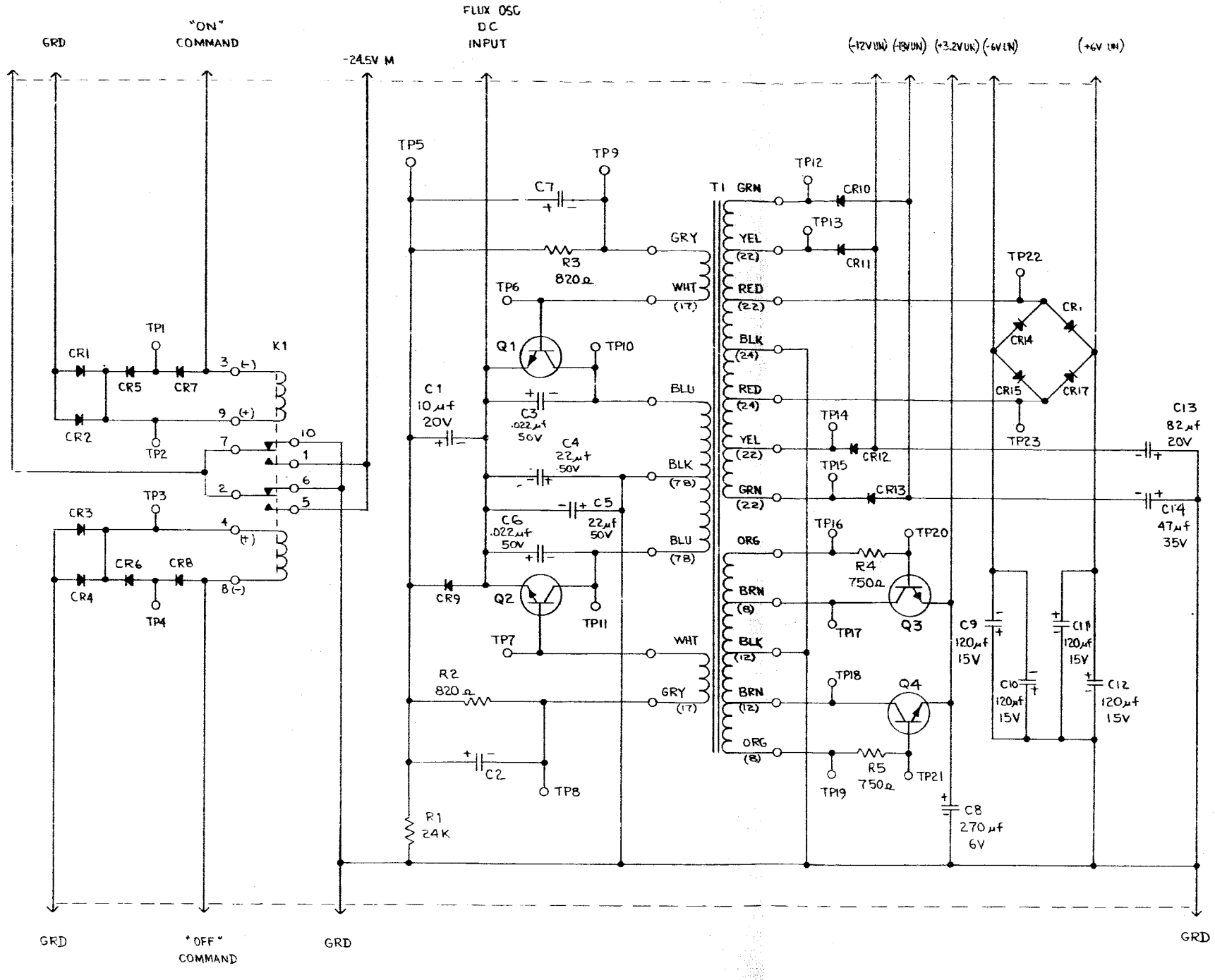
SCALE: NONE
SIZE D
10366-502
DO NOT SCALE THIS DRAWING
WEIGHT
SHEET

See FIGURE 3-1

for

A/D Converter Schematic, No. 10368-502

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	



4. REF ASSY DWG NO. 10369-502
3. CAPACITORS ARE .02 μf 50V
2. TRANSISTORS ARE 2N2658
1. DIODES ARE IN3730
NOTE UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
		LIST OF MATERIAL OR PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: .XX ± .03, .XXX ± .010
ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .1285: +.002, —.001
.136 TO .228: +.003, —.001
.234 TO .500: +.004, —.001
.515 TO .750: +.005, —.001
.765 TO 1.000: +.007, —.001
1.015 TO 2.000: +.010, —.001

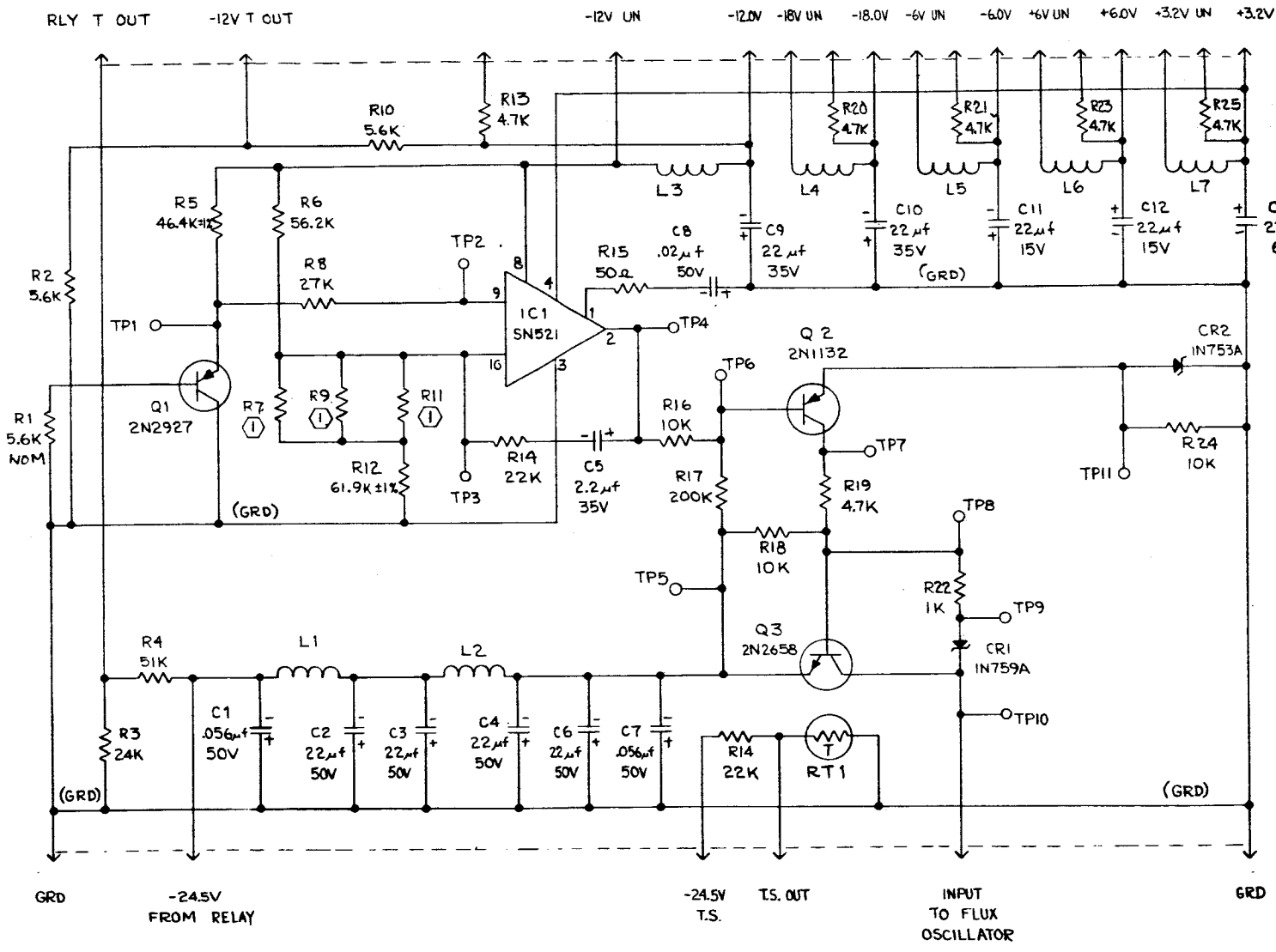
DRAWN	O. HAMPTON	18 JAN, 1966
CHECK		
APPD		
APPD		
FINISH		
HEAT TREAT		
SURFACE ROUGHNESS PER MIL-STD-10	✓	

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC- DC TO DC CONVERTER NO. 1

SCALE:	SIZE	
NONE	D	10369-502
DO NOT SCALE THIS DRAWING	WEIGHT	SHEET

REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	



4. REF ASSY DWG NO. 10371-502
(1) 3. VALUE TO BE DETERMINED AT FUNCTIONAL TEST
2. CHOKES ARE 10 µh.
1. RESISTOR VALUES ±2% ¼w
NOTE: UNLESS OTHERWISE SPECIFIED

REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
LIST OF MATERIAL OR PARTS LIST				

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS: .XX ± .03, .XXX ± .010
ANGLES: ± 0° 30'
DRILLED HOLES
.040 TO .125 +.002 −.001
.136 TO .228 +.003 −.001
.234 TO .500 +.004 −.001
.515 TO .750 +.005 −.001
.765 TO 1.000 +.007 −.001
1.015 TO 2.000 +.010 −.001

DRAWN O. HAMPTON P. JANUSZ
CHECK
APPD
APPD
FINISH
HEAT TREAT
SURFACE ROUGHNESS PER MIL-STD-10 ✓

CALIFORNIA COMPUTER PRODUCTS INC.
305 MULLER, ANAHEIM, CALIFORNIA

SCHEMATIC - DC TO DC CONVERTER NO. 2

SCALE: NONE
SIZE: D
10372-502
DO NOT SCALE THIS DRAWING
WEIGHT
SHEET